MODULE-1

Types of Semiconductor :-

(I) Intrinsic (or pure) Semiconductor
(II) Extrinsic (or Impure) Semiconductor

Intrinsic Semiconductor :-

→ The pure form of semiconductor is known as Intrinsic Semiconductor.
→ But conductivity is very less.
Example - Germanium (Ge), Silicon (Si) etc.

Extrinsic Semiconductor :-

→ The impure form of Semiconductor is Extrinsic Semiconductor.
→ Its conductivity is high (to increase the conductivity of intrinsic Semiconductor some impurity is added and so resultant Semiconductor is impure form.
→ Example : Si + P, Si + B etc.

Formation of electron and Holes pair in Intrinsic Semiconductor

→ The valence band electron can move from valence band to conduction band, when the covalent bond is breaking.
→ The energy required to break a covalent

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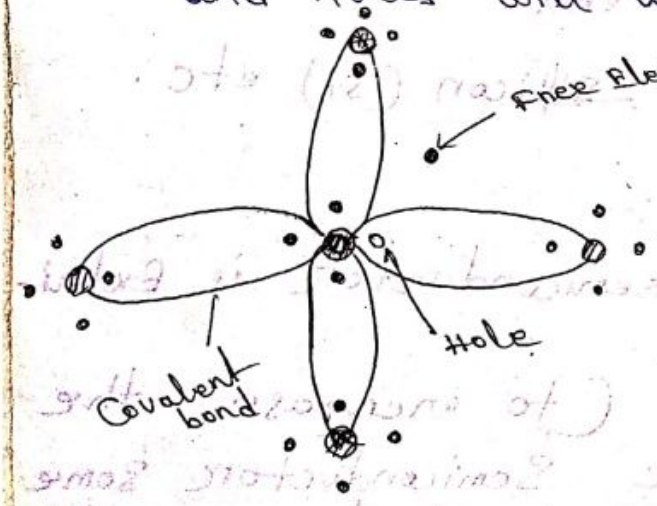
bond the same as Eg (i.e Eg = 0.72 eV for Germanium and 1.12 eV for silicon).

→ This energy may be supplied either by thermal energy or by increasing the temp.

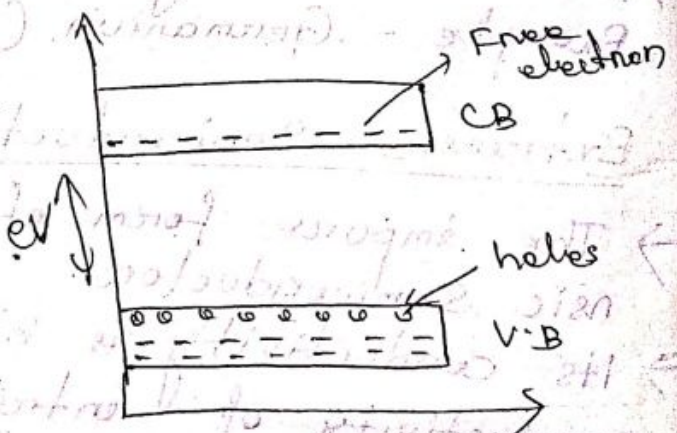
→ When an electron breaks a covalent bond of an intrinsic Semiconductor and moves away and become free, a valency is created in the broken covalent bond.

→ This valence is called hole. Thus free electrons and holes are always generated in pairs.

→ Therefore concentration of free electrons and holes will always be equal in an ISC.



fig(a) crystal structure



fig(b) Energy band diagram

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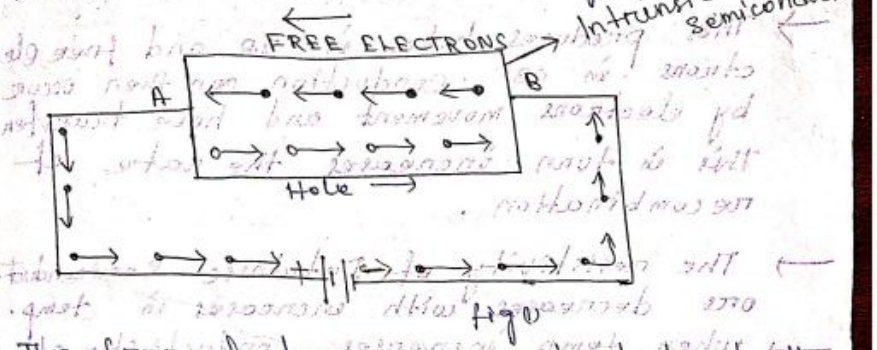
Conduction in Intrinsic Semiconductors

→ In an intrinsic semiconductor, even at room temp, hole electron pairs are created. → when electric field is applied across an intrinsic semiconductor, the current conduction takes place by two process, namely: by free electrons and holes as shown in fig(1)



fig()

→ The free electrons are produced due to the breaking up of some covalent bonds by thermal energy.

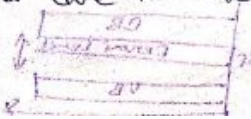
→ At the same time, holes are created ~~due to the breaking up of~~ in the some covalent bonds. ~~by~~

→ Under the influence of electric field, conduction through the semiconductor is by both free electrons and holes.

→ Therefore, the total current inside the semiconductor is the sum of current due to free electrons and holes.

→ It may be noted that current in the external wire is fully electronic i.e by electrons. and hole being positive charged move towards the -ve terminal of battry.

→ Therefore the total current inside the Semiconductor is due to holes and electrons



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Effect of Temp in Intrinsic S.C

→ Since at absolute zero temp no free electrons are available in Intrinsic Semiconductor and it behaves like a perfect insulator.

→ When the Semiconductor is heated, electrons break away from their parent atoms and moves from the V.B to C.B.

→ This produces holes in V.B and free electrons in CB. Conduction can then occur by electrons movement and hole transfer this in turn increases the rate of recombination.

→ The resistivity of Intrinsic Semiconductors decreases with increases in temp.

→ When temp increases, conductivity of pure Semiconductor increases.

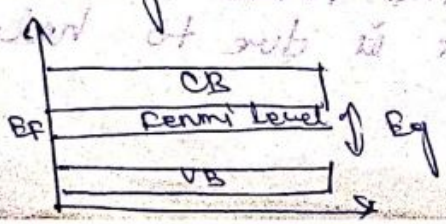
Fermi level in Intrinsic Semiconductor

→ Simply it is a reference energy level at which the probability finding an electron 'n' energy units above it in the conduction band and is equal to the probability of finding a hole 'n' energy units below it in the VB.

→ Thus it can be considered to be average energy level of electrons.

where E_f = Fermi level energy

→ In the Intrinsic Semiconductor the Fermi level lies midway bet^n the CB and VB.



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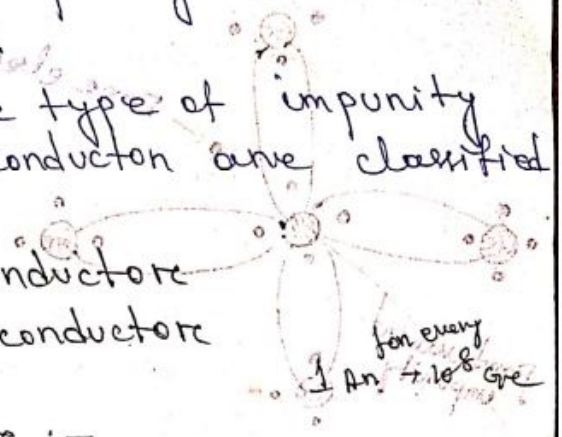
Extrinsic Semiconductor :-

Since an intrinsic semiconductor has less current conduction capable at ordinary room temp.

So to increase the conductivity a very small amount of impurity is added i.e called doping and resultant impurity s.c is called extrinsic semiconductor.

Depending upon the type of impurity added, extrinsic semiconducton are classified into

(I) n-type semiconductor
(II) p-type semiconductor



for every 1 An. 4×10^8 Ge

(I) n-type semiconductor :-

When a small amount of pentavalent impurity ~~is added~~ such as arsenic, antimony, phosphorus is added to pure semiconductor it is known as n-type semiconductor.

→ Since Intrinsic semiconductor atoms have only four electrons and four holes in their valence shells.

→ When a phosphorous pentavalent impurity is added with Intrinsic Semiconductor (such as Si) four electrons are engaged to form covalent bonds with neighbour Si or Ge atoms. remaining one electron as ~~atom~~ free and enters to conduction band of Intrinsic Semiconductor

→ The pentavalent impurity is called as donor type impurity as it donates one electron to the conduction band of pure semiconductor.

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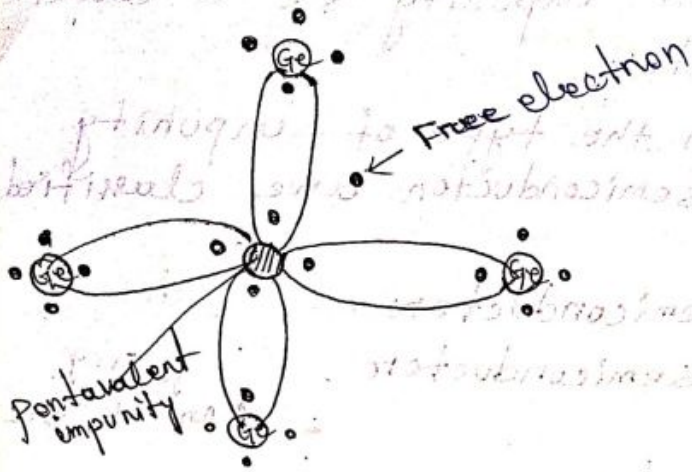
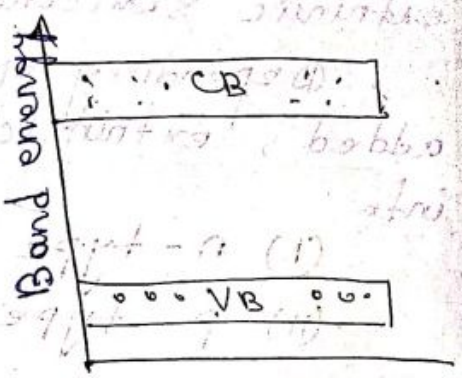
The donor impurity is known as positive ion.

→ Though each impurity provides enough atoms to supply

→ Though each impurity provides only one free electrons yet an extremely small amount of impurity provides enough atoms to supply millions of free electrons.





Energy band diagram

→ Electrical conductivity increases with addition of impurity to Intrinsic semiconductor.

→ In n/t type semiconductor electrons are majority carriers, holes are minority carriers. Because before addition of impurity no of electron = no of holes.

P-type Extrinsic Semiconductor :-

→ When a trivalent impurity (small amount) such as boron, gallium, indium or aluminium is added to a pure semiconductor crystal it called the p-type extrinsic semiconductor.

→ when trivalent impurity is added to silicon or Germanium, these atoms form three complete covalent bond with four surrounding silicon or Germanium atoms by

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shown and one incomplete bond which gives rise to hole.

→ Such impurity atom are available positive carriers because they create holes which can accept electrons.

→ These impurities are consequently known as acceptor impurities.

→ The conductivity increases with addition of more impurity to pure semiconductor.

→ In the p- type semiconductor, holes are majority charge carriers and electrons are minority charge carriers.

Effect of temp on Extrinsic Semiconductor

→ Addition of a small amount of impurity (donor or acceptor) provides large no mobile charge carriers and hence conductivity of Extrinsic semiconductor is many times that of an Intrinsic semiconductor at room temp.

→ If the temp of an Extrinsic (n type) semiconductor is increased the additional thermal energy increases thermally generated carriers. As a result minority concentration (i.e holes) increases.

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→ Eventually a temp is reached called critical temp, then large no of covalent bond are broken so that the no of holes approximately the same as no of electrons.

Now the extrinsic conductors behaves like Intrinsic Semiconductor but with higher conductivity.

Difference betn p-Type and n-Type

p - Type	N - Type
→ It is formed by adding trivalent impurity to intrinsic semiconductor. The trivalent impurities are B, Al, In	→ It is formed by adding pentavalent impurity to intrinsic semiconductor. The pentavalent impurities are P, As, Sb.
→ when trivalent impurity is added, all three electrons take part in bonding, but 4th both remain incomplete.	→ when pentavalent impurity is added, 4 of its outermost electrons take part in bonding while one electron remain free.
→ To complete the bond, an electron is borrowed from neighbour creating a hole	
→ Here mavority carriers are holes while minority are electron.	→ Here mavority are electron and minority are holes.
→ As mavority carriers are tuely charged (hole) so it is p-type	→ As mavority are tuely charged (electron) so it is n-type
~~1/2~~ Ge atom ton eleny 108 si atom	1 As atom for every 10^8 si atom

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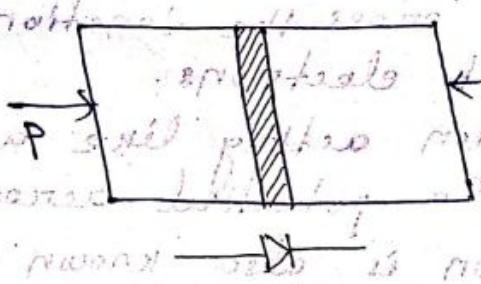
PN JUNCTION DIODE :-

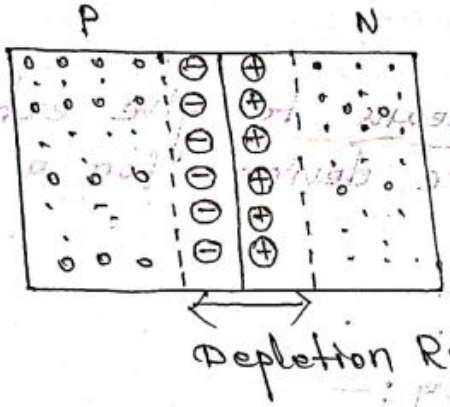
→ When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called pn Junction.

→ Technique of doping :- Ion implemetation.

→ In metal, no barrier present in pn Junction a barrier is there which makes it special.



Formation of PN Junction :-



→ N type has majority electrons while minority carriers are ~~electrons~~ holes.

→ P- type has majority carriers as holes, and minority carriers as electrons.

→ So there is a concentration difference of carriers on either side of Junction.

→ Due to this, ~~process~~, ~~& road~~ electrons on N-side have a tendency to move to p-side and holes on p-side have tendency to move to n-side.

→ By this process, +ve ions are generated on N-side and -ve ions are generat

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on p-side, near the junction.

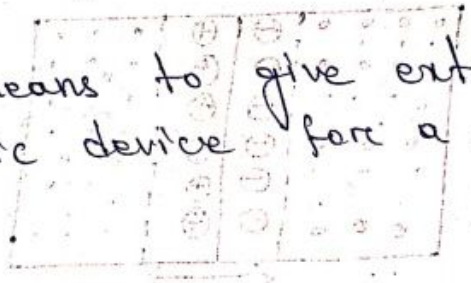
→ so there is a region created near the junction, only consisting of immovable ions i.e depleted or absence of movable carriers (or mobile charge carriers) so this region is known as depletion region.

→ The +ve ions on n-side restrict the holes on p-side to cross the junction, similar is the case of electrons.

→ so this region acting like a barrier by creating a potential across the Jun" so this region is also known as potential barrier.

BIASING :-

Biasing means to give external dc to an electronic device for a defined operation.



Types :-

(1) Zero Biasing :-

when no dc voltage is applied across the terminals of a p-n junction diode the barrier potential doesn't allow flow of charge carriers, Hence the net diode current is 0 (zero).

(2) Forward Biasing :-

→ This is said to be forward biased if p-type is connected to +ve terminal and n-type is connected to -ve terminal of the supply.

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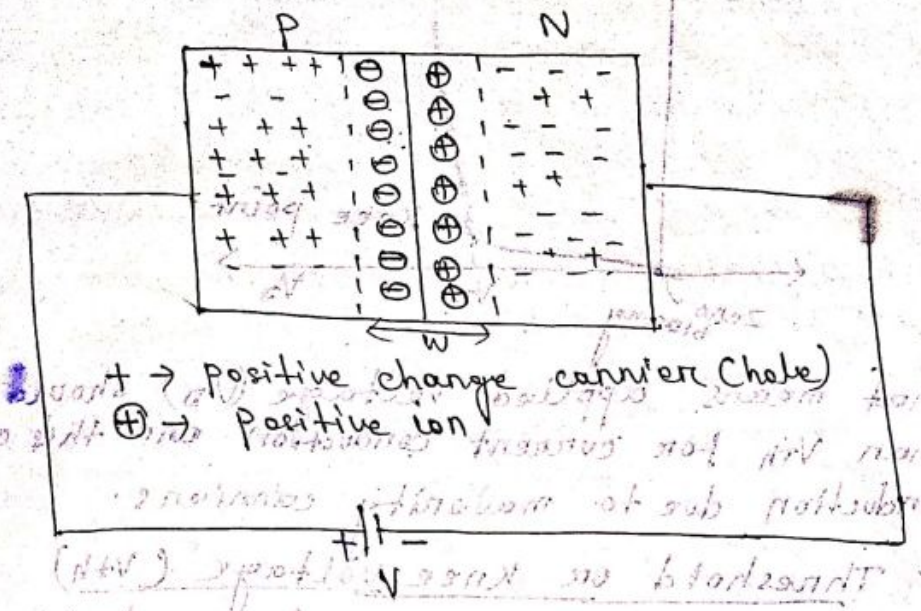

→ So -ve terminal of applied voltage repells the -ve charge carriers (electrons) in N region and move towards the junction and +ve terminal repells the +ve charge carrier (hole) in P- region and move towards junction.

→ As a result when applied voltage is more than internal barrier potential (V_{th}) at the depletion region; the potential barrier vanishes.

→ So finally electron can reach at +ve terminal of supply and hole can reach at -ve terminal means current conduction occurs.

→ At junction depletion region disappears means resistance is very less as in forward bias condn.

→ So due to repulsion forces at junction, the width of depletion region decreases and at a particular voltage, the depletion region vanishes and there is sharp rise in current which indicates resistance is very less. This voltage is known as threshold (V_{Th}) knee voltage.

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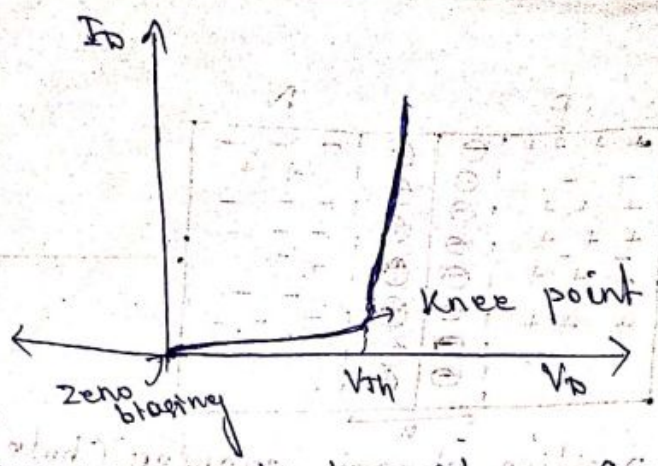


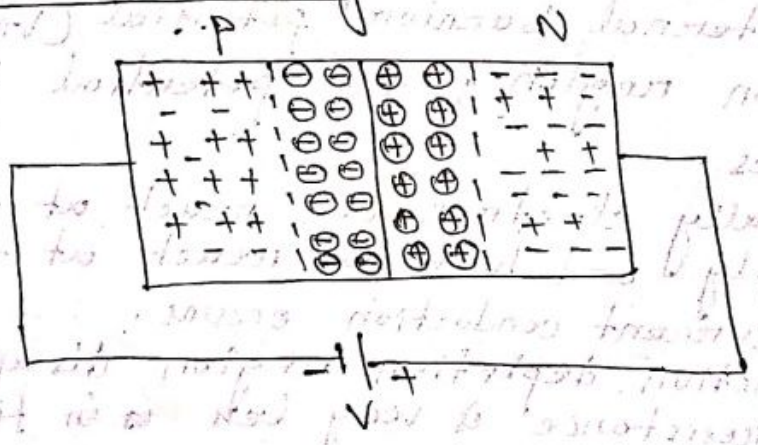
→ That means applied voltage (V_D) should more than V_{th} for current conduction and this current conduction due to majority carriers.

Note Threshold or Knee Voltage (V_{th})

It is the minimum forward bias voltage at which diode starts conducting or there is exponential growth in diode current.

V_{th} (Si) ≈ 0.7V
V_{th} (Ge) = 0.3V.

(3) Reverse Biasing :—



→ The diode is said to be reverse biased if p-type is connected to -ve terminal and n-type is connected to +ve terminal of the supply.

→ Due to connection of +ve terminal to n-type, the electrons are attracted towards the +ve terminal and similarly holes towards the -ve terminal.

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→ As a result +ve ions in N-region and -ve ions in p-region increases which strengthen the depletion region becomes wider.

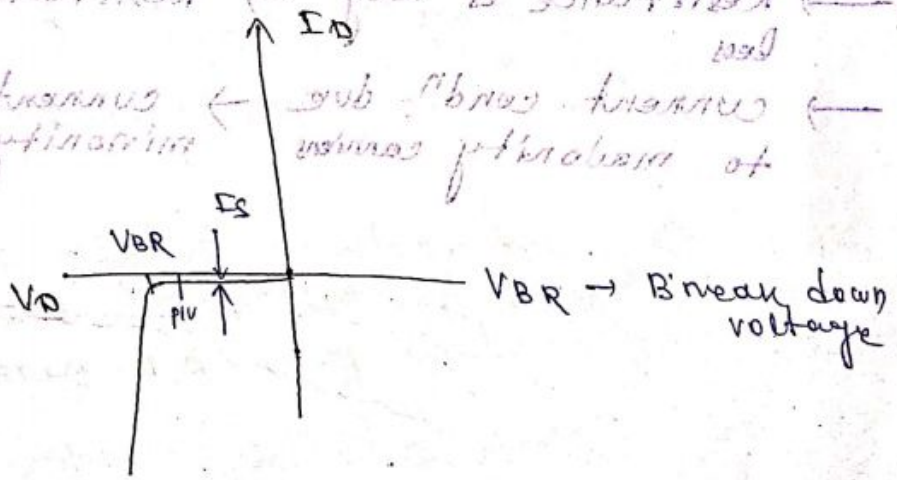
→ So at Junction in N-region side +ve ions and -ve ions in p-region sides increases.

→ So further movement of electrons and holes N-region to p-region and vice versa becomes not possible due to +ve ion repels holes and -ve ion repels electron in corresponding region. So potential barrier increases

→ As a result no current flows due to majority carriers.

Reverse saturation current :-

Theoretically no current should flow in external circuit but in practice a very small current (in range of micro Ampere) flows due to minority carriers i.e known as leakage current or reverse sat^n current.



Breakdown voltage :-

The min reverse bias voltage after which there is an exponential growth in reverse current is called Breakdown voltage.

At this voltage, normally diodes burns out or permantely damaged.

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Peak Inverse Voltage (PIV) :-

It is the max reverse bias voltage that the diode can withstand without getting damaged.

that is specified by manufacturer.

Comparision :-

Forward Bias	Reverse Bias
→ Connection of +ve terminal to p-type and -ve terminal to n-type	→ connection is just opposite.
→ More forward current flows	→ No current flows but very less leakage current (reverse sat^n current) flows
→ Thin depletion region produced	→ wider depletion region.
→ Resistance is very less	→ Resistance is very hi
→ current condn due to majority carriers	→ current condn due to minority carriers.

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Mobility (μ) :-

It is defined as the drift velocity per unit electric field strength.

or

It is the ability of movement of carriers, like electrons and holes.

If μ_n or μ_e → mobility of electron

or μ_p or μ_h → mobility of holes

Then $\mu_n > \mu_p$

$$\mu = \frac{V_d}{\vec{E}}$$

V_d → drift velocity

$\vec{E}$ → Electric field

Its unit m^2/Volt-sec.

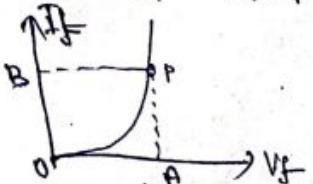
Resistance of a crystal diode

Generally semiconductor has two resistance. Forward and reverse resistance

Forward Resistance :-

when a diode is forward biased, the resistance offered by the diode to the flow of current is known as R_F. It is very small and the diode act as short cut element. It is two types

(a) Dc forward resistance :-



when dc supply is applied across a diode the resistance offered by the diode to the path of direct current flow is known as dc forward resistance

$$\text{d.c forward resistance, } R_f = \frac{OA}{OB}$$

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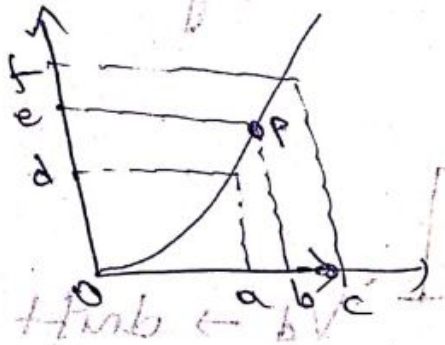
(ii) ac forward resistance

It is the opposition offered by the diode to the changing forward current.

It is measured by the ratio of change in voltage across diode to the resulting change in current through it i.e

ac forward resistance, r_f = Change in forward voltage / Change in forward current



$$\frac{\Delta V}{\Delta I} = \frac{bc - ba}{bf - bd} = \frac{ae}{df}$$

Break Down :-

The phenomenon in reverse biasing at which increase of reverse voltage the reverse current increases rapidly as a result breakdown occurs.

Types

(a) Avalanche breakdown
(b) Zener Breakdown

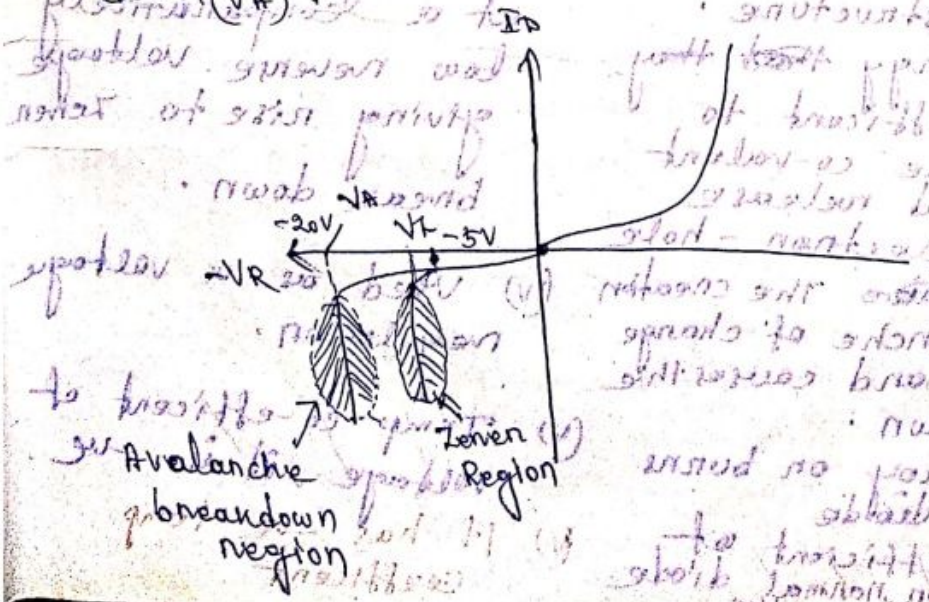
(a) Avalanche breakdown :-

→ In the reverse bias cond^n when the voltage across the diode is increased the velocity of minority carriers will increase.

→ Then the associated kinetic energy (ie $K.E = \frac{1}{2}mv^2$) will be sufficient to release additional carriers through collisions.

→ That is ionization process will result whereby the valence electrons absorbs sufficient energy to leave the parent atom.

→ This is a cumulative process which is referred as avalanche multiplication which results the flow of large reverse current (avalanche current) which find avalanche breakdown (V_A).



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(b) Zener Breakdown :-

→ When the p and n-type materials are highly doped in reverse biased a strong electric field is produced.

→ Because of existence of strong electric field in the region of junction, the covalent bonds breaks within the atom and results more carriers. So reverse current increases in the breakdown region.

→ Under such circumstances, this is refered as zener breakdown and vied diode is called zener diode.

Avalanche Breakdown	Zener Breakdown
(i) Occurs in normally doped diodes	(i) Occurs in very heavily doped diode.
(ii) $V_{breakdown} = -20V$	(ii) $V_{zener\ Break} = -5V$
(iii) High velocity, minority carriers with sufficient Ek cross the depletion layer and collides with crystal structure. → The energy they is sufficient to break the co-valent bonds and release extra electron-hole pairs. The creation of avalanche of charge carriers and causes the breakdown.	(iii) The intense electric field of reduced depletion layer tears apart the crystal structure at a comparatively low reverse voltage giving rise to zener breakdown.
(iv) It destroy or burns out the diode	(iv) Used as a voltage regulator.
(v) Temp co-efficient of voltage for normal diode it is +ve	(v) Temp co-efficient of voltage is -ve
	(vi) It has -ve temp coefficient

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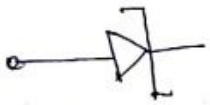
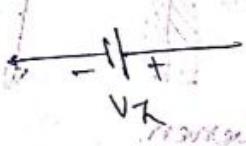
Zener Diode :-

→ It is highly doped than ordinary diode
→ It is used in breakdown region which is capable of more power dissipation.
→ Operation of a zener diode is same as that of ordinary pn diode under forward biased condition but its speciality is it is also operated in reverse biased cond?.
→ So zener diode is preferrably used in reverse biased mode operation.
→ Its symbol is a Z from the word zener,



(Symbol)



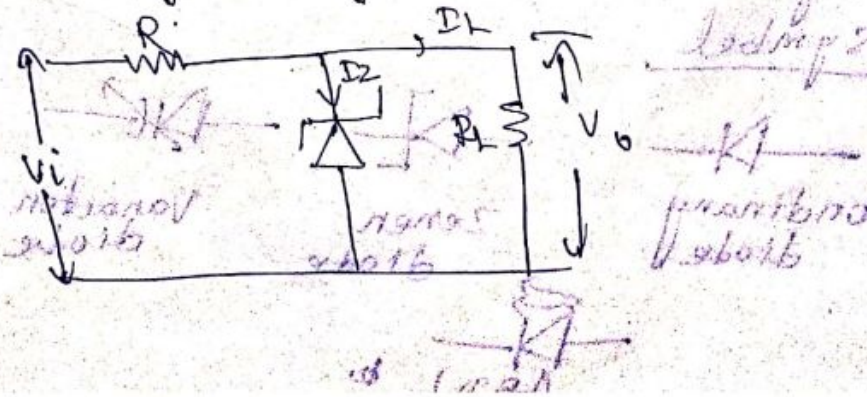
(Equivalent ckt)

VI Characteristics of zener Diode

When applied voltage is greater than Vz (zener breakdown voltage) it is 'ON' state otherwise 'OFF'.

Use

Zenere diode are used most frequently as a voltage regulator (or reference voltage)



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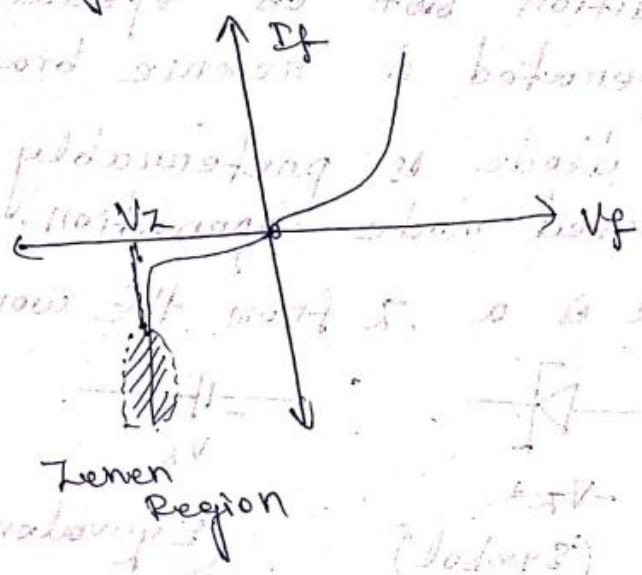
How it act as regulator :-

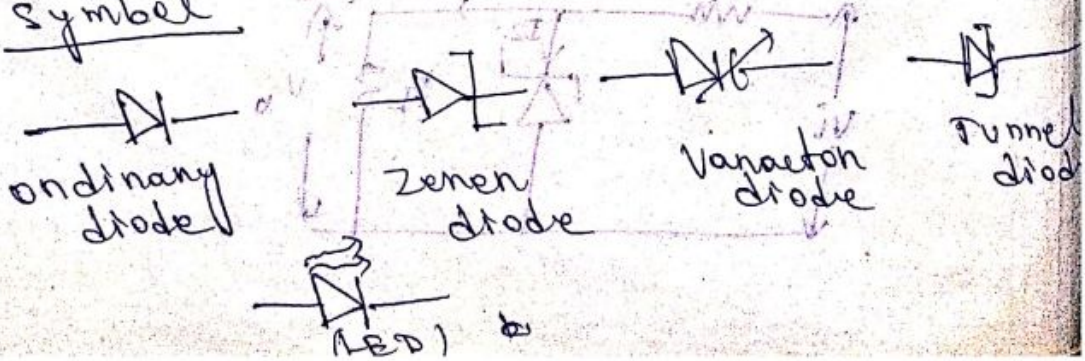
→ Under reverse bias condition, the voltage across the diode remains almost constant although the current through the diode increases. So it is used as voltage regulator.



→ Because it provides constant voltage across the load (R_L) whereas input voltage may be varying over a range.

→ As shown in V-I characteristics curve of zener diode, as long as input voltage does not fall below V_z, the voltage across the diode will be constant and hence the load voltage will be constant.

Symbol



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APPLICATION OF DIODE

Rectification :-

The process of converting ac to pulsating dc is known as rectification and the device is known as rectifier.

Types :-

(I) Half wave rectifier
(II) Full wave rectifier

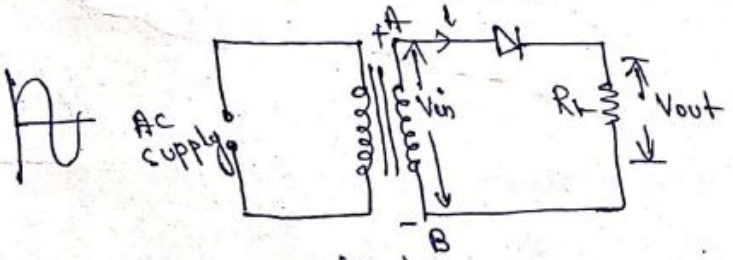
(I) Half wave rectifier :-

→ In half wave rectification, the rectifier conducts current only during the +ve half cycles of input a.c supply.

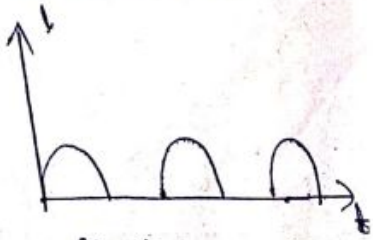
→ The -ve half cycles of a.c supply are suppressed i.e during -ve half cycle, no current is conducted, and hence no voltage appears across the load.

→ So current flows in one direction (i.e dc) through the load after every half cycle.

Circuit diagram :-



fig(i)



fig(ii)

Operation :-

The a.c voltage across the secondary winding AB changes polarities after every half cycle During the +ve half-cycle of input a.c voltage, end A becomes positive w.r.to end

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This makes the diode forward biased and hence it conducts current. During the -ve half cycle, end A is negative w.r.to end B.

→ Under this condition, the diode is reverse biased and it conducts no current.

→ Therefore, current flows through the diode during positive half cycle of input a.c voltage only; it is blocked during the -ve half cycle which is shown in fig A(ii)

→ In this way current flows through load R_L always in the same direction. Hence dc o/p is obtained across R_L.

Note: The output across the load is pulsating dc. These pulsations in the output are further smoothened with the help of filter ckt.

Disadvantages:-

(i) The pulsating current in the load contain alternating component whose basic frequency is equal to the supply frequency. Therefore, an elaborate filtering is required to produce steady direct current.

(ii) The a.c supply delivers power only half the time. Therefore o/p is low.

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Efficiency of Half-wave Rectifier

The ratio of d.c power output to the applied input a.c power is known as rectifier efficiency i.e

$$\text{Rectifier efficiency, } \eta = \frac{\text{d.c power o/p}}{\text{Input a.c power}}$$

d.c power :-

The output current is pulsating dc. Therefore, in order to find d.c power average current has to be found out.

$$I_{av} = I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i\,d\theta = \frac{1}{2\pi}\int_0^{\pi} \frac{V_m \sin\theta}{r_f + R_L}\,d\theta$$

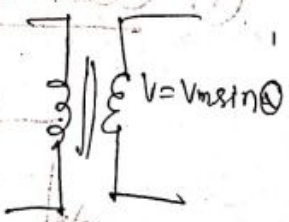
$$= \frac{V_m}{2\pi(r_f+R_L)}\int_0^{\pi} \sin\theta\,d\theta$$

$$= \frac{V_m}{2\pi(r_f+R_L)}\left[-\cos\theta\right]_0^{\pi}$$

$$= \frac{V_m}{2\pi(r_f+R_L)} \times 2$$

$$= \frac{V_m}{(r_f+R_L)} \times \frac{1}{\pi}$$

$$= \frac{I_m}{\pi} \qquad \left[\because I_m = \frac{V_m}{r_f+R_L}\right]$$



d.c power, $P_{dc} = I_{dc}^2 \times R_L = \left(\frac{I_m}{\pi}\right)^2 \times R_L$

a.c power input :-

The a.c power input is given by

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

For half wave rectifier wave, $I_{rms} = I_m/2$

$$P_{ac} = \left(\frac{I_m}{2}\right)^2 \times (r_f + R_L)$$

$$\text{Rectifier efficiency} = \frac{\text{d.c o/p power}}{\text{d.c i/p power}} = \frac{(I_m/\pi)^2 \times R_L}{(I_m/2)^2 (r_f+R_L)}$$

$$= \frac{0.406\,R_L}{r_f+R_L} = \frac{0.406}{1+\frac{r_f}{R_L}}$$

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The efficiency will be maximum if r_f is negligible as compared to R_L.

∴ Max. rectifier efficiency = 40.6%.

9| Full wave Rectifier :-

A full wave rectifier utilises both half cycles of input ac voltage to produce the d.c output.

The following two circuits are commonly used for full wave rectification.

(I) Centre-Tap fullwave rectifier
(II) Full wave bridge rectifier

(I) Centre-Tap fullwave rectifier

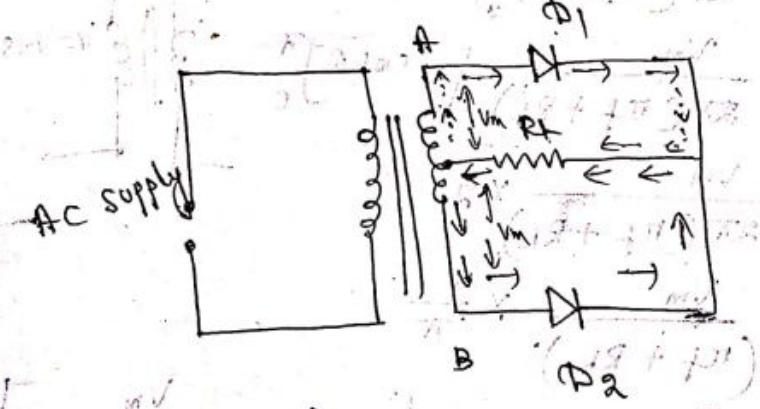

Fig 2(A)

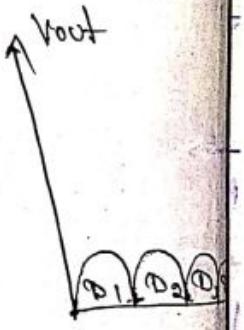

Fig 2(b)

→ The circuit employs two diode D1 and D2 as shown in the above fig. A center tap secondary winding AB is used with two diodes connected so that each uses one half-cycle of input a.c voltage.

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Operation :-

→ During the +ve half-cycle of secondary voltage, the end A of the secondary winding becomes positive and end B negative.

→ This makes the diode D_1 forward biased and diode D_2 reverse biased.

→ Therefore, diode D_1 conducts while diode D_2 does not

→ The conventional current flows is through diode D_1, load resistor R_L and the upper half of secondary winding as shown by the dotted arrows.

→ During the -ve half cycle, end A of the secondary winding becomes -ve and end B positive.

→ Therefore, diode D_2 conducts while diode D_1 does not.

→ The conventional current flow is through diode D_2, load R_L and lower half winding as shown by solid arrows. Refering to fig 2(A)

→ It may be seen that current in the load R_L is in the same direction for both half cycles of input a.c voltage.

Peak inverse voltage

$$PIV = 2V_m$$

Disadvantages :-

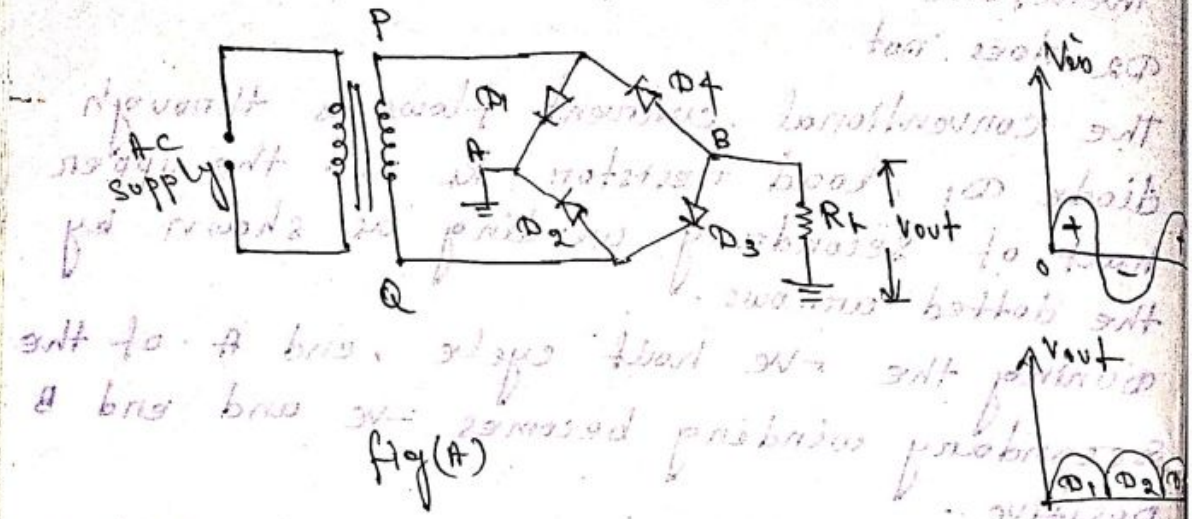
(i) It is difficult to locate the centre tap on the secondary winding.

(ii) The d.c output is small as each diode

Utilise only one half of the transformer secondary voltage.

(iii) The diode used must have high peak inverse voltage.

(ii) Full wave Bridge Rectifier :-



fig(A)

→ The need for a centre tapped power transformer is eliminated in the bridge rectifier.

→ It contains four diodes D_1, D_2, D_3 and D_4 connected to form bridge as shown in fig

→ The ac supply to be rectified is applied to the diagonally opposite ends of the bridge through the transformer. Between other two ends of the bridge, the load resistance R_L is connected

Operation :-

→ During the half cycle of secondary voltage, the end P of the secondary winding becomes +ve and end Q negative.

→ This makes diodes D_1 and D_3 forward biased while diode D_2 and D_4 are reverse biased.

→ Therefore, only diodes D_1 and D_3 conduct.

→ The conventional current flows is shown by dotted arrows in fig (B).

It may be seen that the current flows from A to B through R_L.

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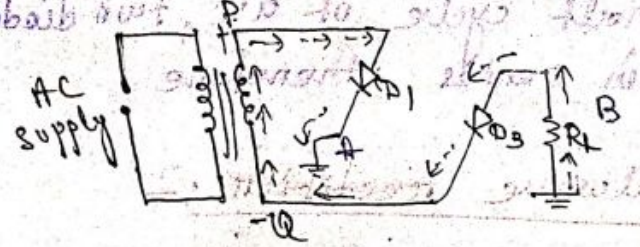
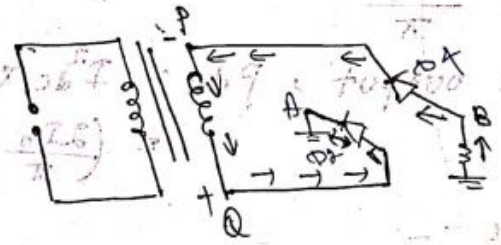


fig(B)

→ During the -ve half cycle of secondary voltage end P becomes negative and @ end Q positive.

→ This makes diode D_2 and D_4 forward biased whereas diodes D_1 and D_3 are reverse biased.

→ Therefore D_2 and D_4 conducts. The current flow is shown by solid arrows. in fig(C)



fig(C)

→ It may seen that again current flows from A to B through the load R_L. i.e in the same direction as for the half cycle.

→ Therefore dc o/p is obtained across the load R_L

Peak inverse voltage :-

$$PIV = V_m$$

Advantages :-

(i) The need for centre tapped transformer is eliminated.

(ii) The output is twice that of the centre tap circuit for the same secondary voltage.

(iii) The PIV is one half that of centre tap ckt

Disadvantages :-

→ It requires 4 diodes.

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→ As during each half cycle of a.c input, two diodes that conduct are in series, therefore,

Efficiency of fullwave rectifier :-

Let $v = V_m \sin\theta$ be the a.c voltage to be rectified. Let r_f and R_L be the diode resistance and load resistance respectively.

d.c output power

$$I_{dc} = \frac{2I_m}{\pi}$$

∴ d.c power output, $P_{dc} = I_{dc}^2 \times R_L$

$$= \left(\frac{2I_m}{\pi}\right)^2 \times R_L$$

a.c input power :-

The a.c input power is given

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

For fullwave rectified wave, we have

$$I_{rms} = I_m/\sqrt{2}$$

$$P_{ac} = \left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)$$

∴ Full wave rectification efficiency is

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{(2I_m/\pi)^2 R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)}$$

$$= \frac{8}{\pi^2} \times \frac{R_L}{(r_f + R_L)}$$

$$= \frac{0.812 R_L}{r_f + R_L} = \frac{0.812}{1 + \frac{r_f}{R_L}}$$

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The efficiency will be maxm if r_f is negligible as compared to R_L.

∴ Maximum efficiency = 81.2%.

This is double the efficiency due to half wave rectifier. Therefore, a full wave rectifier is twice as effective as a half wave rectifier.

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BIPOLAR JUNCTION TRANSISTOR (BJT)

Introduction :-

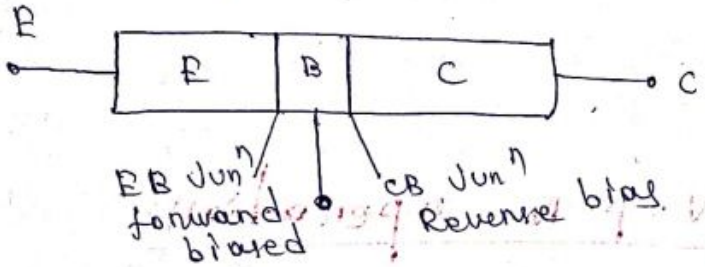
Defi - Transistor can be defined as a 3 terminal device where a p-type material is sandwitched betⁿ two n-type materials or vice-versa.

→ It is a current controlled device.
→ It is used as an Amplifier.
→ Its input resistance is is less and output resistance is very high.

Use

→ Satelite
→ Mobile phones
→ High speed switches

Construction :-



→ It is a three terminal device (Emitter, Base and collector).

Emitter :-

→ It is heavily doped.
→ ~~Doping change~~
→ Funⁿ of Emitter is to inject charge carrier into Base.
→ Its length is more than base but less than collector.

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Base :-

→ It is the middle region of the device
→ It is very thin.
→ It is lightly doped
→ Base fun^{n} is to pass all change carrier from emitter to collector.

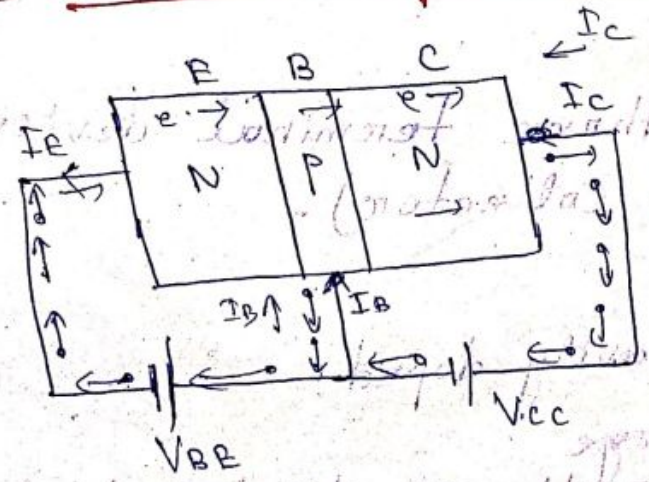
Collector :-

→ It is the outer region.
→ Its width is more compare to emitter and base.
→ Its fun^{n} is to collect the change carriers
→ Its width or length is highest because all change carriers are collected which may produce more heat ; so to dissipate heat its size is bigger.

Types

① N-P-N
② P-N-P

① N-P-N operation



fig(1) Basic connection of npn transistor

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Working of npn transistor :-

→ Fig(i) shows the npn transistor with forward bias to emitter base junction and reverse bias to collector - base junction.

→ The forward bias causes the electrons in the n-type emitter to flow towards the base.

→ This constitute the emitter current I_E. As these electrons flow through the p-type base, they tends to combine with hole.

→ As the base is lightly doped and very thin, therefore, only a few electrons (less than 5%) combine with holes to constitute base current I_B.

→ The remainder (more than 95%) cross over into the collector region to constitute collector current I_C.

→ In this way, almost the entire emitter current flows in the collector ckt. It is clear that emitter current is the sum of collector current and base current

$$I_E = I_B + I_C$$

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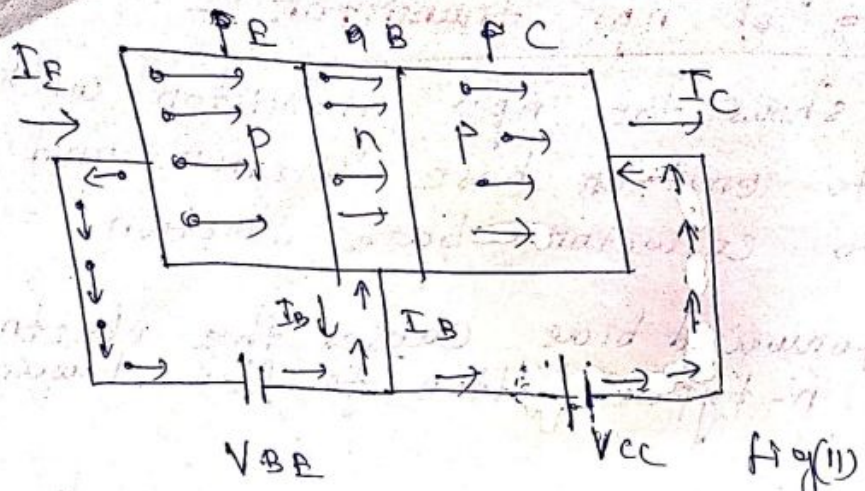
(11) P-N-P Operation :-



Fig(11)

→ Fig(11) shows the basic connection of a pnp transistor → The forward bias causes the holes in the p-type emitter to flow towards base.

→ This constitute the emitter current I_E. As these holes cross into n-type base, they tend to combine with the ~~holes~~ electrons.

→ As the base is lightly doped and very thin, therefore, only a few holes (less than 5%) combine with the electrons.

→ The remainder (more than 95%) cross into the collector region to constitute collector current I_C.

→ In this way, almost the entire emitter current flows in the collector ckt.

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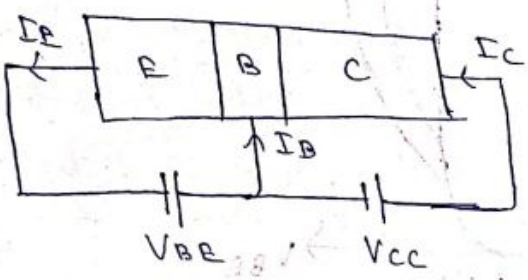
Types of configuration :-

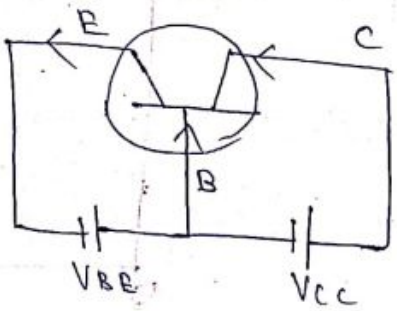
(I) Common Base configuration (CB).
(II) Common Emitter configuration (CE)
(III) Common collectore configuration (CC)

(I) CB configuration :-

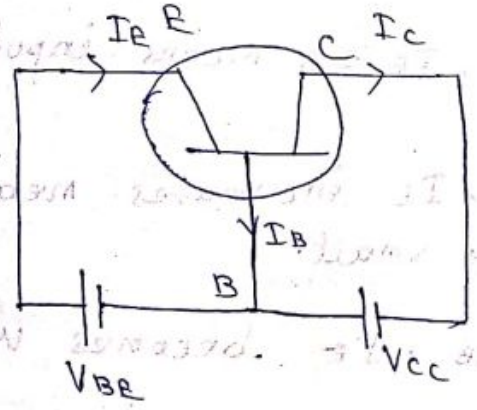
Here Base is common to both input and o/p.



Notation



(Symbol for N-P-N)



Symbol (P-N-P)

Note For NPN :- I_C and I_B always inward to transistor and direction of I_E always outwards.

For P-N-P :- I_C and I_B always outward and I_E inward.

In both the cases, $I_E = I_B + I_C$ must be satisfied.

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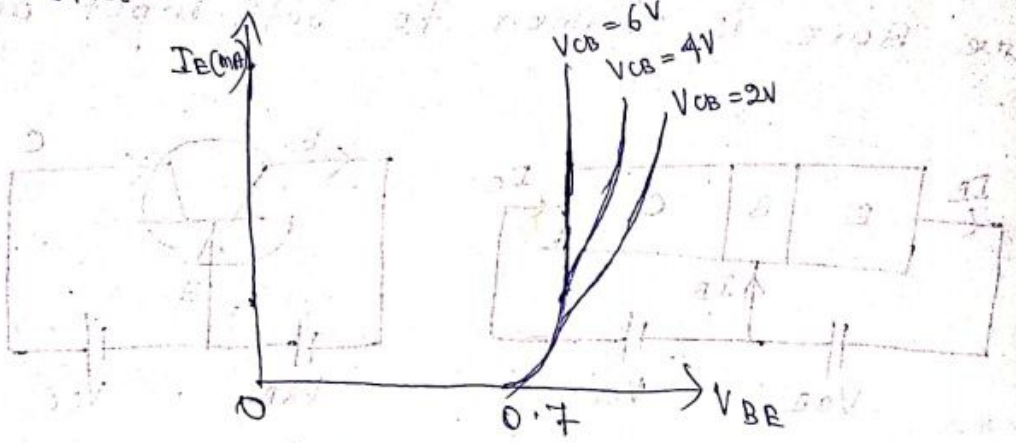
Characteristics of CB transistor :-

Input characteristics :-

→ The curve plotted bet^n input current (I_E) and input voltage (V_{BE}) at constant output voltage (V_{CB}) is called input characteristics.



→ Input resistance $r_i = \frac{V_{BE}}{I_E}$ | at constant V_{CB}

→ Before $V_{BE} = 0.7V$, $I_E \cong 0$ means input current is very less.

→ when V_{BE} increases, I_E increases means input resistance is very small.

→ with increase of V_{CB}, I_E becomes very

Output characteristics

→ The curve plotted bet^n o/p current (I_C) and o/p voltage (V_{CB}) at constant input current (I_E) is called o/p characteristics.

→ Output resistance, $r_o = \frac{V_{CB}}{I_C}$ | at cont I_E

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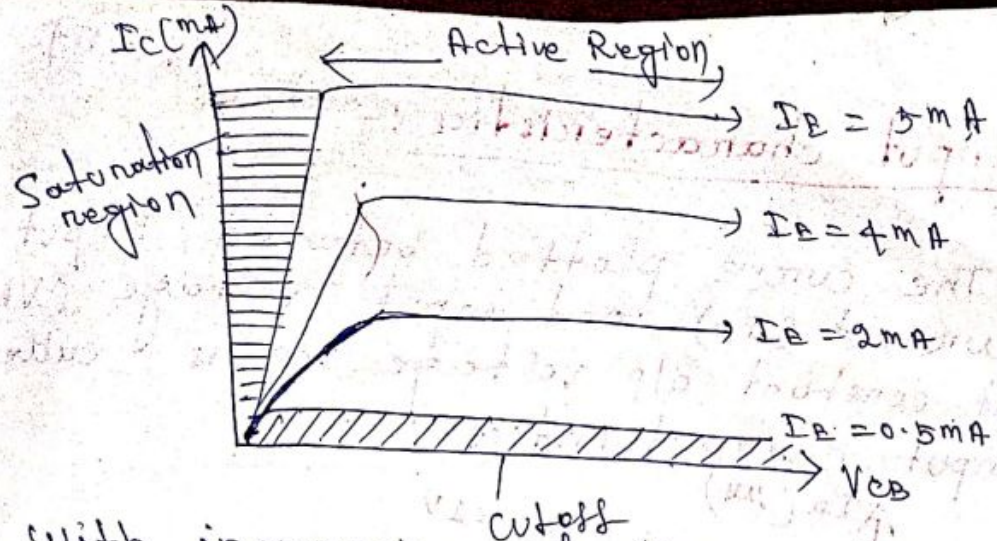
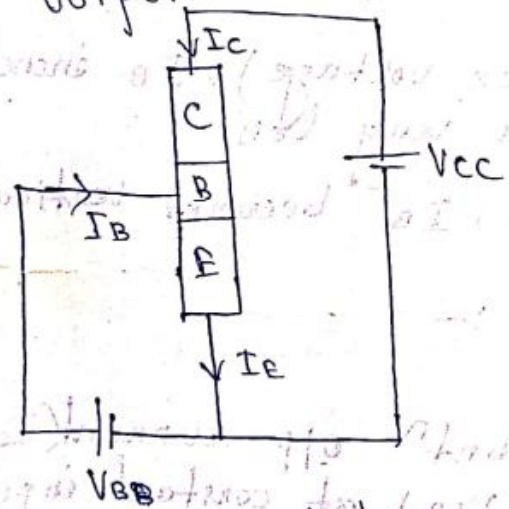


→ With increasing of V_{CB}, I_C increases very slow and becomes float means o/p resistance r_o is very high.

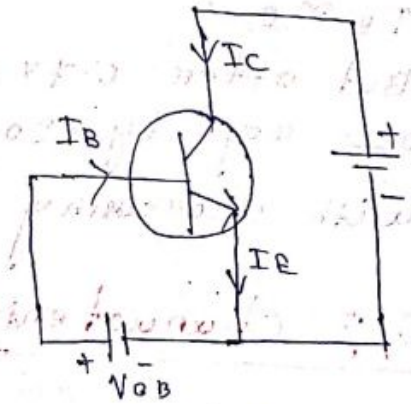
→ If V_{CB} is -ve, o/p side becomes forward biased (as input side), I_C increases rapidly, at this cond^n I_C is independent of I_B.

Characteristics of CE configuration:-

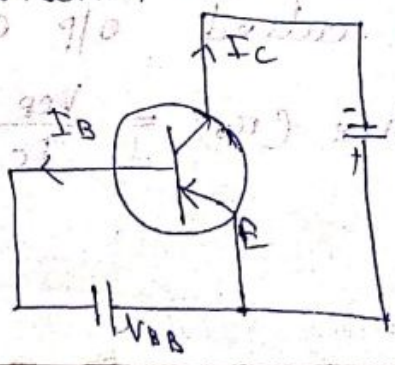
Here Emitter is common to both input and output.



Notation



(Symbol N-P-N type)



(Symbol P-N-P type)

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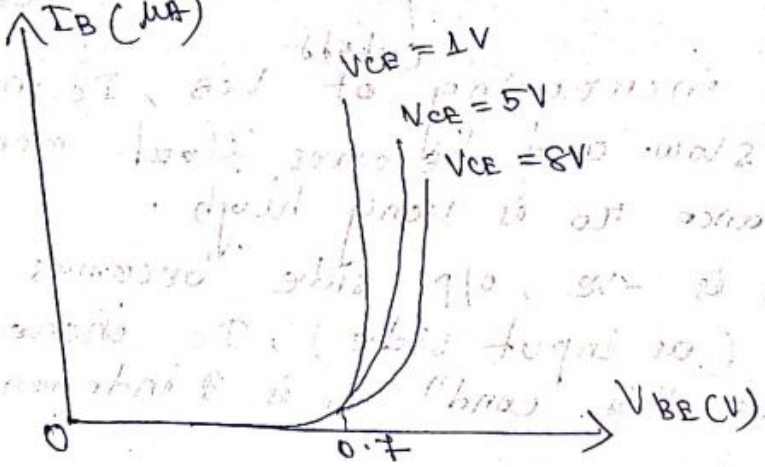
Input characteristics :-

→ The curve plotted between Input current (I_B) and input voltage (V_{BE}) at constant o/p voltage V_{CE} is called input characteristics.



→ Input resistance (r_i) = $\frac{V_{BE}}{I_B}\Big|_{V_{CE}\ \text{const}}$

→ Before $V_{BE} = 0.7$, the input current $I_B \cong 0$

But after 0.7V (Knee voltage), I_B increases rapidly so r_i is very less.

→ With decreasing V_{CE}, I_B becomes vertic

O/p characteristics :-

→ The curve plotted bet" o/p current(I and output voltage (V_{CE}) at constant inp current (I_B) is called o/p characteristi

→ Output resistance (r_o) = $\frac{V_{CE}}{I_C}\Big|_{I_B\ \text{constant}}$

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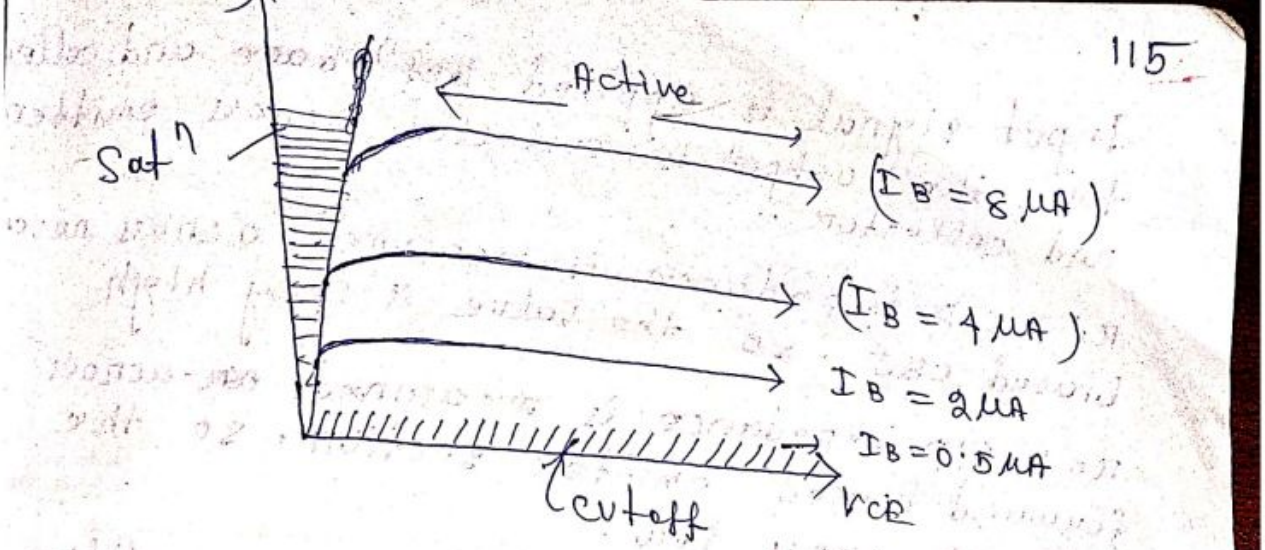
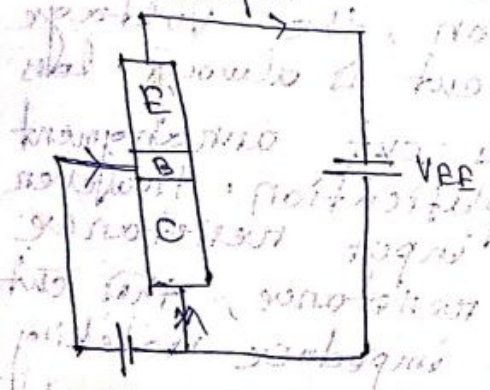


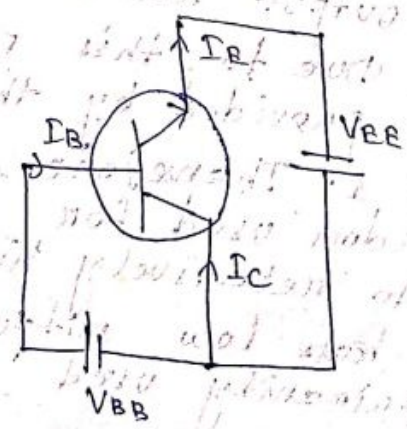
→ With increasing of V_{CE}, I_C increases very slow and curve is flat (but not exactly flat) and less flat comparie to CB configuration.

(iii) Common collector configuration :-

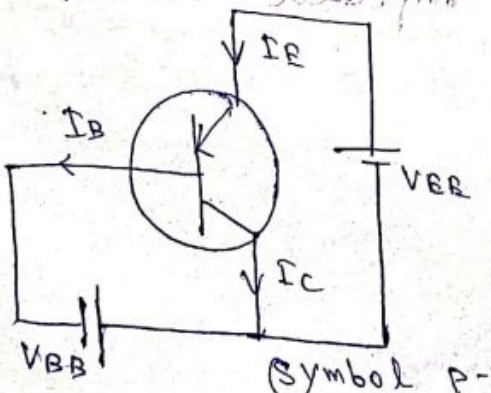
Here collector is common to both input and output.



(Notation)



Symbol (N-p-N)



(Symbol p-N-p)

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Input signal is applied bet^n base and collector, the output is collected across emitter and collector.

r_i : I/p impedance is measured across reverse biased CBJ. so the value is very high

r_o : O/p impedance is measured across forward biased Emitter section. so the value is very low.

So it is not suitable for an amplifier design.

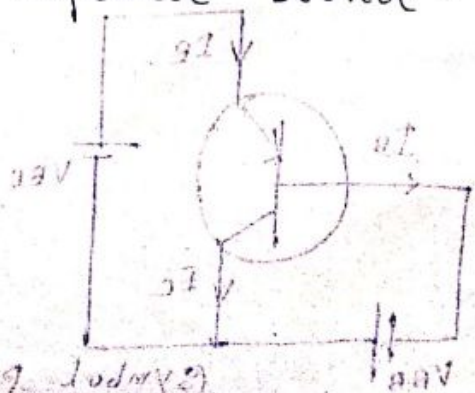
Application :-

→ Impedance matching.
→ It compesates the resistance mismatch.

(or)

The common collector circuit has very high input resistance (about 750kΩ) and very low output resistance (about 25Ω).

Due to this reason, the voltage gain provided by this ckt is always less than 1. Therefore, this ckt arrangement is seldom used for amplification. However due to relatively high input resistance and low output resistance, this ckt is primarily used for impedace matching i.e for driving a low impedace load from a high impedace source.



Comparision among CB, CE and CC

Current amplification factor :-

For CB

It is the ratio of o/p current to I/p current.

current amplification factor, $\alpha = \frac{I_C}{I_E}$

$$\Rightarrow \boxed{I_C = \alpha I_E}$$

This is due to majority carrier only.

$\boxed{I_C = \alpha I_E + I_{CBO}}$ when leakage current is considered

I_{CBO} : collector to Base minority current when emitter terminal is opened and it occurs due to reversed biased. This leakage current is very small.

$$\boxed{I_{CBO} = I_{CO}}$$

Generally $\alpha < 1$ ($\alpha = 0.9$ to 0.99)

For CE

Current amplification factor, $\beta = \frac{I_C}{I_B}$

$$\Rightarrow \boxed{I_C = \beta I_B}$$

It is due to majority carriers only.

$\boxed{I_C = \beta I_B + I_{CEO}}$ when leakage is considered

I_{CEO} : collector to emitter current when base is opened, and it occurs due to reverse biased and it is leakage current, which is very small.

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I_C (Total) $= I_{Cmaj} + I_{Cmin}$

$\Rightarrow I_C = \alpha I_E + I_{CBO}$

I_{CBO} → Leakage current by minority carr due to ~~reversed~~ biased o/p junction never biased.

$\Rightarrow I_C = \alpha (I_C + I_B) + I_{CBO}$ $(\because I_E = I_C + I_B)$

$\Rightarrow I_C (1-\alpha) = \alpha I_B + I_{CBO}$

$\Rightarrow I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \frac{I_{CBO}}{1-\alpha}$

$\left[\because \frac{\alpha}{1-\alpha} = \beta \text{ and } \frac{1}{1-\alpha} = \beta + 1\right]$

$\Rightarrow \boxed{I_C = \beta I_B + (\beta+1) I_{CBO}}$

CC : current amplification factor $= \gamma$

$\gamma = \frac{I_E}{I_B}$ (ratio of o/p current to I/P current)

$\Rightarrow I_E = \gamma I_B$

Generally γ

Relationship among α, β, γ

$I_E = I_C + I_B$

$\Rightarrow \frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$ (deviding I_C in both sid

$\Rightarrow \left(\frac{1}{\alpha}\right) = 1 + \left(\frac{1}{\beta}\right)$

$\Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}}$ and $\boxed{\alpha = \left(\frac{\beta}{1+\beta}\right)}$

$I_E = I_C + I_B \Rightarrow I_E = \beta I_B + I_B \Rightarrow I_E = (\beta+1) I_B$

Also $I_E = \gamma I_B$ (from cc) — (ii)

from (i) and (ii), $\boxed{\gamma = \beta + 1} = \left(\frac{\alpha}{1-\alpha}\right) + 1 = \frac{1}{1-\alpha}$

Finally, $\gamma = (\beta+1) = \left(\frac{1}{1-\alpha}\right)$

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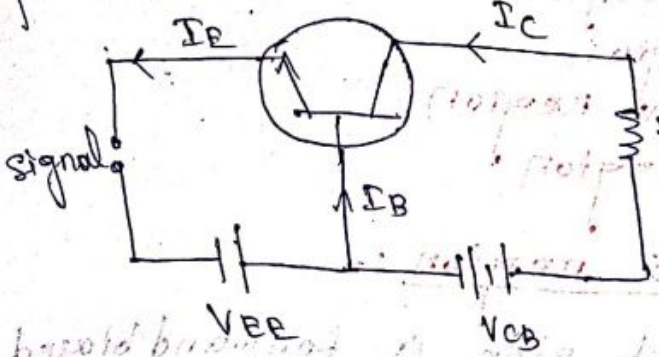
Transistors circuit as an Amplifier

→ A transistor raises the strength of a weak signal and thus acts as an amplifier.

→ Fig(A) shows the basic circuit of a transistor amplifier.



Fig(A).

→ The weak signal is applied b/t emitter-base junction and output is taken across the load R_C connected in the collector ckt

→ In order to achieve faithful amplification, the input circuit should always remain forward biased

→ To do so a d.c voltage is applied in the input ckt in addition to the signal as shown.

→ This dc voltage is known as bias voltage and its magnitude is such that it always keeps the input ckt forward biased.

→ As the input circuit has low resistance, therefore, a small change in signal voltage causes an appreciable change in emitter current.

→ This causes almost the same change in collector current due to transistor action.

→ The collector current flowing through a high load resistance R_C produces a large voltage across it.

→ Thus a weak signal applied in the input circuit appears in the amplified form in the collector ckt. In this way transistor act as an amplifier.

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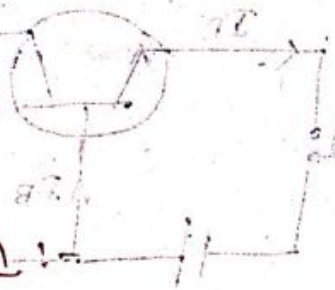
Operation Mode of a transistor

A transistor is operated in active region.

Types of region

(I) Active region
(II) Saturation region
(III) cutoff region



(I) Active region :-

→ When input side is forward biased and output side is reversed.

→ Actually in this region transistor operates

(II) Saturation region :-

→ When both input and output side forward biased.

→ In this case current becomes max^m

→ In this region a transistor is operated in 'ON' mode.

(III) Cutoff Region :-

→ When both input and output side are reversed biased.

→ In this current is zero (minimum).

→ In this case a transistor is operated in ~~(II)~~ 'OFF' mode

* So a transistor is used as a switch because it can be operated in 'ON' mode (in sat^n region) and it can be operated in 'OFF' mode (cutoff region) so to work and OFF it act as a switch

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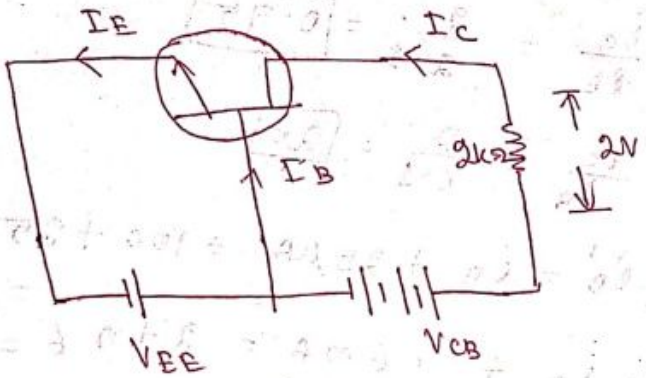
Example

In a common base connection, $\alpha = 0.95$. The voltage drop across 2kΩ resistance which is connected in the collector is 2V. Find the base current.



fig(1)

Soln

Fig(1) shows the required common base connection. The voltage drop across R_C (=2kΩ) is 2V.

$$\therefore I_C = 2V / 2K = 1\,mA$$

$$\alpha = I_C / I_E$$

$$I_E = \frac{I_C}{\alpha} = \frac{1}{0.95} = 1.05\,mA$$

Using the relation, $I_E = I_B + I_C$

$$I_B = I_E - I_C = 1.05 - 1$$

$$= 0.05\,mA$$

Problem

A transistor has $i_B = 100\,\mu A$ and $i_C = 2\,mA$, find α and β of the transistor. If i_B changes by $+25\,\mu A$ and i_C changes by $+0.6\,mA$, find the new value of β.

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Soln

$i_B = 100\,\mu A = 0.1\,mA$

$i_C = 2\,mA$

$i_E = i_B + i_C = 0.1 + 2 = 2.1\,mA$

(i) $\alpha = \frac{i_C}{i_E} = \frac{2}{2.1} = \boxed{0.95}$

$\beta = \frac{i_C}{i_B} = \frac{2}{0.1} = \boxed{20}$

(ii) Now $i_B' = i_B + 25\,\mu A = 100 + 25 = 125\,\mu A$
$= 0.125\,mA$

$i_C' = i_C + 0.6\,mA = 2 + 0.6 = 2.6\,mA$

$\beta' = \frac{i_C'}{i_B'} = \frac{2.6}{0.125} = \boxed{20.8 \simeq 21}$

Comparision of Transistor Connections

Sl.No	characteristics	CB	CE	CC
1.	Input resistance	low (about 100Ω)	low (about 750Ω)	very
2.	output resistance	very high (about 450K)	High (about 45K)	
3.	Voltage gain	about 150	about 500	
4.	Application	For high frequency	For audio frequency	
5.	Current gain	less than 1	High (β)	

MODULE-2

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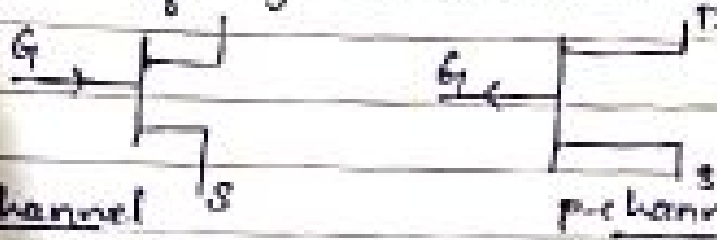
Field Effect Transistor →

FET is a voltage controlled current device in which drain current (I_D) is controlled by gate to source voltage (V_{GS}).

FET may be classified as → n channel FET
p channel FET

n-channel FET is preffered to p-channel FET because mobility of e⁻s is more than that of holes, so the conductivity of n-channel FET is more than p-chanel FET.



In FET, current is due to the majority charge carrier which is responsible for channel only.

Comparison between BJT and FET →

* BJT is bypolar ie. current is due to both the e⁻s and holes. So, noise is due to both e⁻ and hole but FET is unipolar hence current is due to only one charge carrier so noise is due to only 1 charge carrier for which FET is less noisy compared to BJT.

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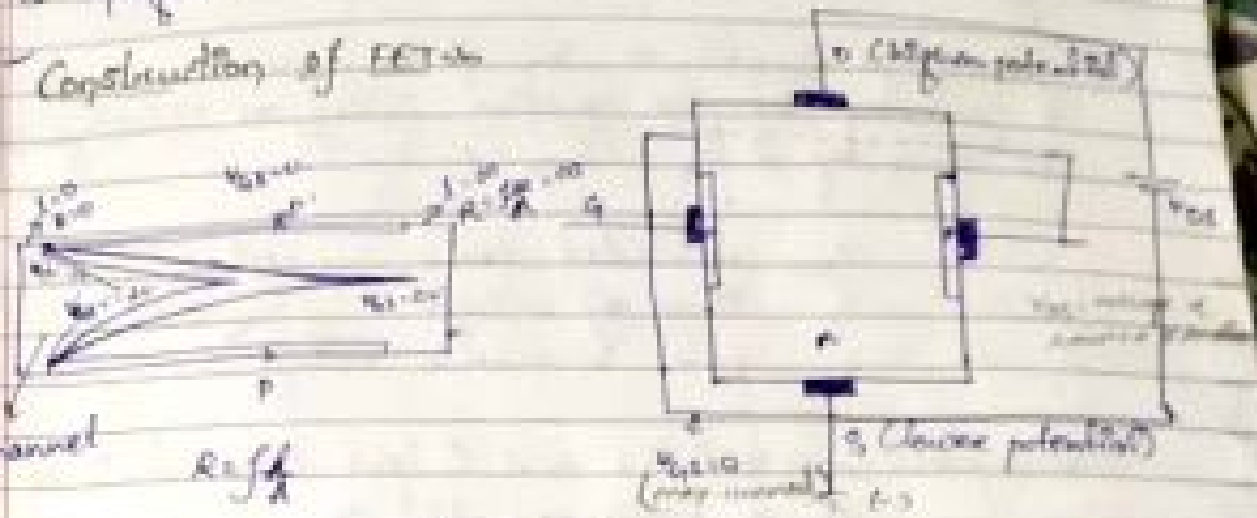
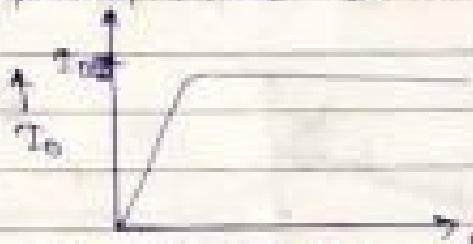
* FET is having highest input impedance component in BJT because by biasing V_{GS} we are maintaining gate as open circuit.
* FET is used as excellent signal chopper (the level of signal is changed)

Construction of FET:-



* The drain current is controlled by applied reverse bias voltage between gate and source terminal
* After setting a V_{GS} value we have to apply V_{DS} between source and drain which must be forward bias to pull the charge carriers from source to drain.
* For a particular V_{GS}, if we increase V_{DS} then drain current increases to a maximum value till it's saturated (Channel)



* When $V_{GS}=0$, the constriction of channel occurs just at the end of the channel, so effective channel for conduction is max so, we get max drain current $I_D = I_{DSS}$ (I_{DSS} = Saturated drain current)

* When V_{GS} is reverse bias mode, the width of the depletion layer increases and as a result constriction of channel occurs away from the channel end. So effective channel length for conduction decreases, so drain current decreases.

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* Pinch-off voltage :- It's the reverse bias voltage at which drain current is 0. ($I_D = 0$)
At pinch off voltage conduction of channel occures at the starting of the channel & other words, effective channel for conduction is almost 0.

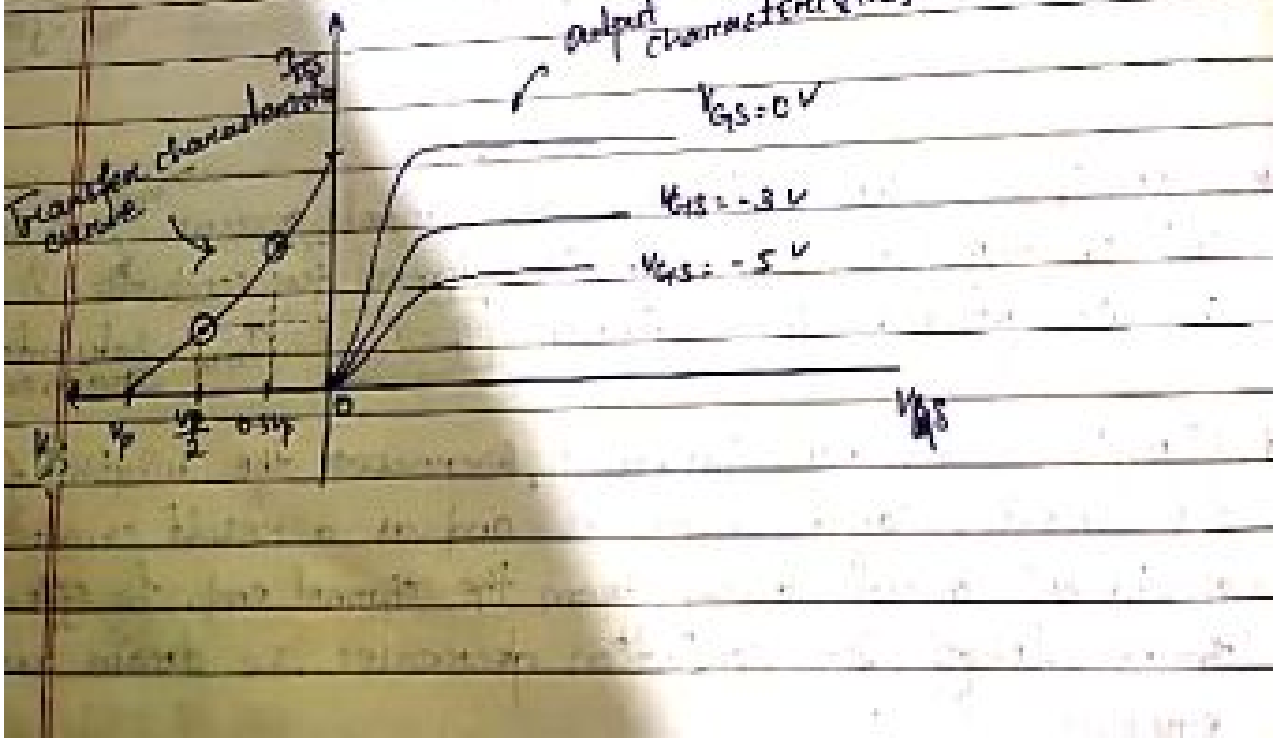
Shockleys Equation :- The drain current of a FET is governed by the equation called as Shockleys eq^n It's given by :- $\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$

I_{DSS} - Saturated drain current
V_P = Pinch off voltage
V_{GS} = Gate to source voltage

Transfer Characteristics and Output Characteristics of a n-channel FET :-

Transfer characteristics :- Transfer characteristics curve is governed by Shockley's equation.

If $V_{GS} = 0$, $I_D = I_{DSS}$ mA
$V_{GS} = V_P$, $I_D = 0$ mA
$V_{GS} = \frac{V_P}{2}$, $I_D = \frac{I_{DSS}}{4}$ mA
$V_{GS} = 0.3 V_P$, $I_D = \frac{I_{DSS}}{2}$ mA



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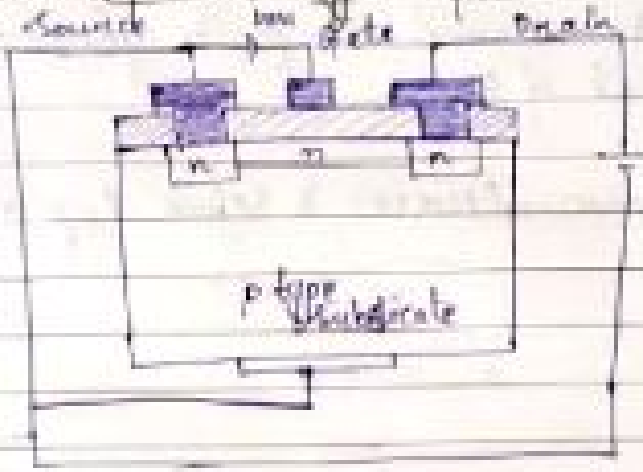
Metal oxide semiconductor field effect transistor (MOSFET)

MOSFET is a three terminal device having the terminal source, drain and gate in which source and drain are separated from gate by introducing materials called as SiO_2 layer.
The purpose of isolating the terminals is to provide high input impedance.
The MOSFET can be as n-channel MOSFET or p channel MOSFET.
The MOSFET can be operated in the following modes
Depletion mode
Enhancement mode

n-channel depletion type MOSFET:-



Operation:- When V_{GS} is zero we will get maximum conducting of the channel because no holes will be entering from substrate to form recombination with the e^- in channel so by increasing V_{DS} we can get maximum drain current I_{DSS}.
If we increase V_{GS}, then due to the -ve terminal of the gate holes we will attracted from the substrate towards the channel as a result recombination occurs, so current decreases due to the application of V_{DS}.
When $V_{GS} = V_p$, the recombination is more so the conduction of the channel is almost 0.

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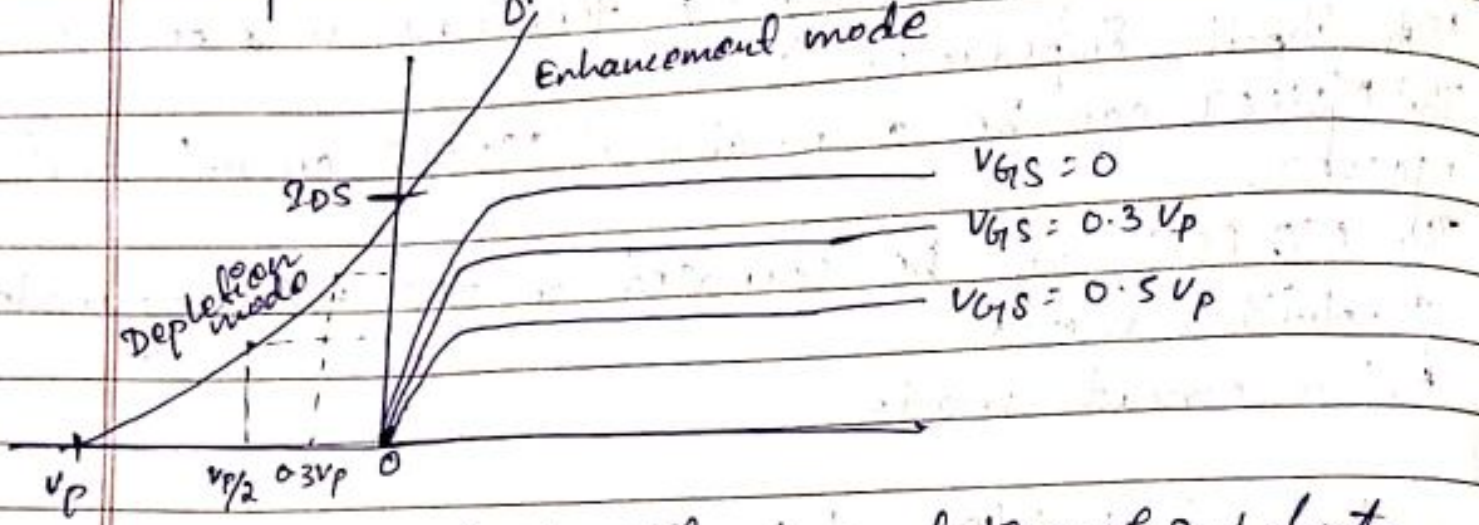
In depletion type MOSFET channel already exists.
If a small +ve V_{GS} is applied to depletion type MOSFET, then the drain current increases drastically, so it's not advisable to operate a depletion type MOSFET in enhancement mode.



NOTE→ Due to the implementation of substrate the effective channel length is greater than that of FET.

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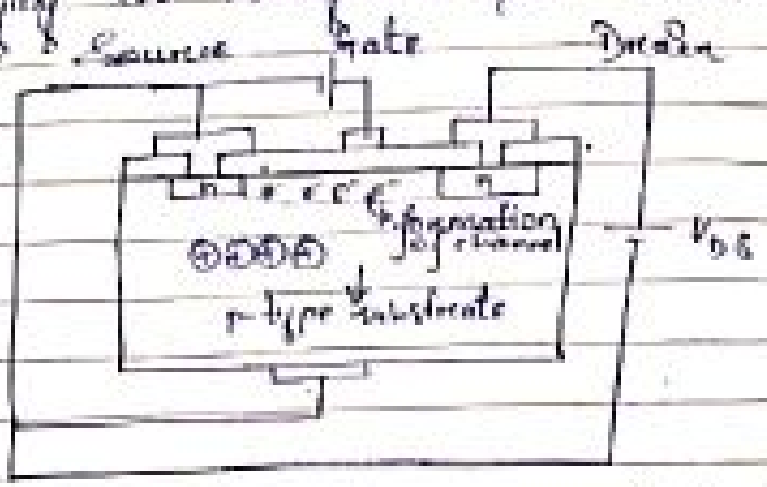
CLASS NOTES

N-channel Enhancement type MOSFET :-

In enhancement it is to be created artificially by applying +ve voltage to gate terminal.

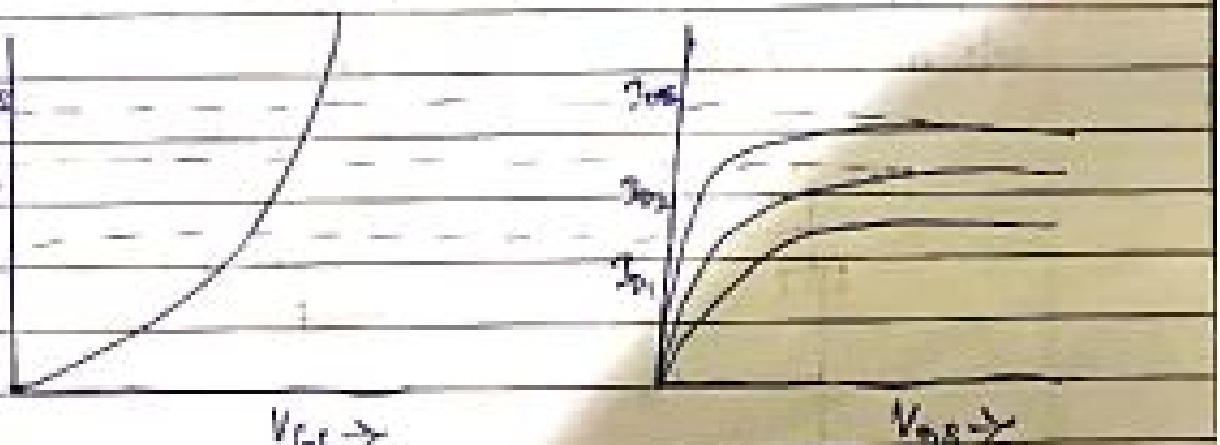


If V_{GS} increases in +ve magnitude then minority e's from substrate will be collected below the SiO$_2$ layer between source and drain to form channel. Channel is formed after a certain voltage for V_{GS} called as "Threshold voltage". So, if V_{GS} is greater than then channel is formed.

So the drain current of an enhancement type MOSFET is governed by the formula.

$$I_D = K[V_{GS} - V_t)^2$$

Where $K = \frac{I_{D(on)}}{(V_{GS(on)} - V_t)^2}$



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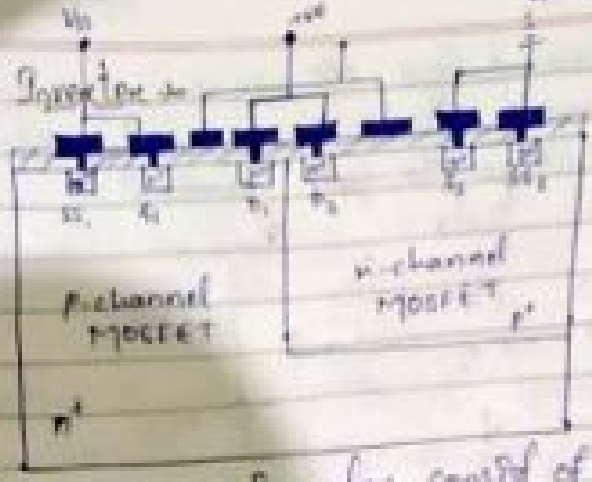
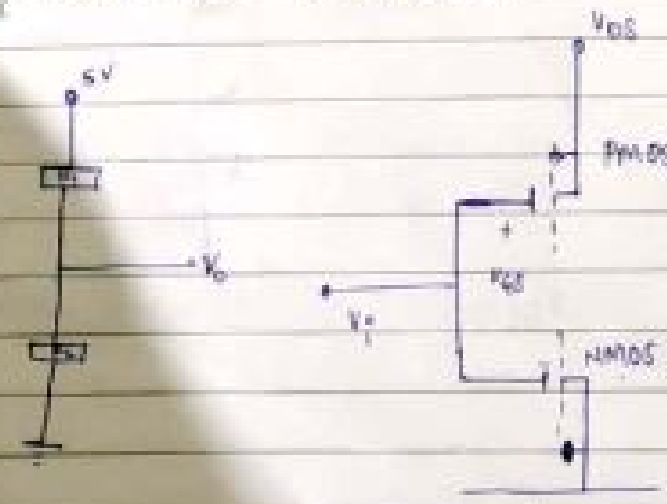
CMOS Inverter



Operation :- CMOS inverter consist of one p-channel and n-channel MOSFET.

* The MOSFETS are basically enhancement type MOSFET where channel is to be formed by applying voltage to the gate terminal of the CMOS inverter.
* When +ve voltage is triggered to the gate terminal then it attracts electron to the source terminal and repel holes towards the substrate.
* As both source and drain are p-type material hence channel is not formed so, pmos is in Off state.
* Similarly, If +ve voltage is applied to the nMOS it will attract e's from the substrate towards the source terminal so, as both source and drain are n+ material hence channel is formed so, nMOS is in ON state.
* Similarly, If -ve voltage is applied the PMOS is in ON state and nMOS is in OFF state so, the CMOS acts as/works like a Inverter.



When -5V is applied to the gate terminal we have

$-5V - V_{GS} = 0 \Rightarrow \boxed{V_{GS} = -5V}$ ∴ NMOS is OFF

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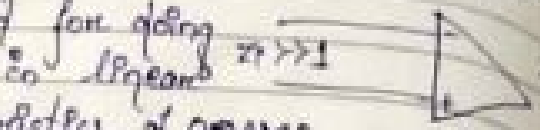
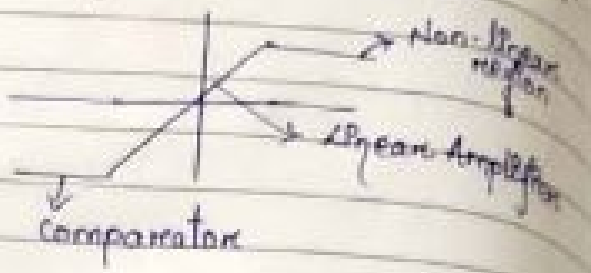
MODULE-3

Operational Amplifier (OPAMP) :-

Operation Amplifier (OPAMP) is a directly coupled high gain differential amplifier having high input impedance and low output impedance.

Initially OPAMP was used for doing mathematical operations in linear region in V-I characteristics of OPAMP but later logical operations was also compiled in non-linear region of V-I characteristics curve.



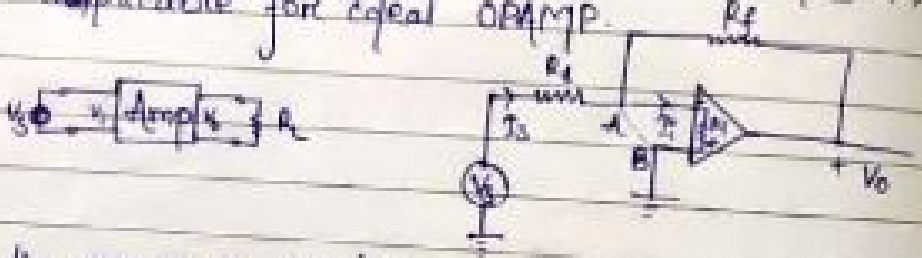


Characteristics Of an Ideal OPAMP :-

* Input impedance must be infinity ($Z_i = \infty$)
* Output impedance should be 0 ($Z_o = 0$)
* Voltage gain must be infinity ($A_v = \infty$)
* Band width must be infinity ($B_{w} = \infty$)
* CMRR = ∞

Virtual Ground or Virtual Short circuit condition :-

It's applicable for Ideal OPAMP.



As the OPAMP is ideal hence $A_v = \infty$

$\Rightarrow \frac{V_o}{V_i} = \infty$

As V_o cant be ∞, hence to make $A_v = \infty$ we have to take $V_i = 0 \Rightarrow R_1 I_f = 0 \Rightarrow I_f = \frac{0}{\infty} \Rightarrow \boxed{I_f = 0}$

I_f can be 0 if we short the terminal A & B of the OPAMP. this concept is called virtual ground or virtual short circuit condition.

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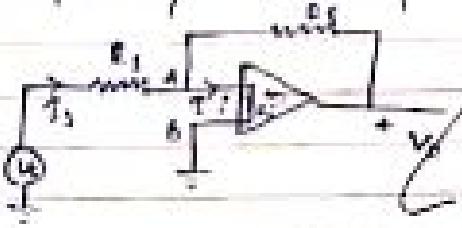
Types of OPAMP :- Taking the source into consideration OPAMP can be classified as :-

* Inverting OPAMP :- If the source is connected to inverting or -ve terminal of the OPAMP then it's called as Inverting OPAMP.

If we consider OPAMP as ideal then we can short the terminal A & B by virtual ground concept & we virtual short circuit condition.

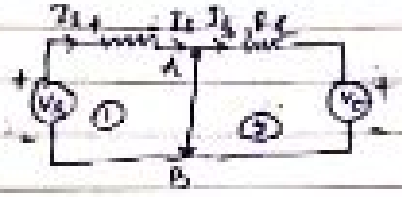


The analysed ideal OPAMP can be expressed as follows :-

From loop ① we have

$$+V_s - I_s R_1 = 0$$

$$\Rightarrow \boxed{I_s = \frac{V_s}{R_1}} \rightarrow ①$$



From loop ② we have

$$-I_s R_f - V_o = 0$$

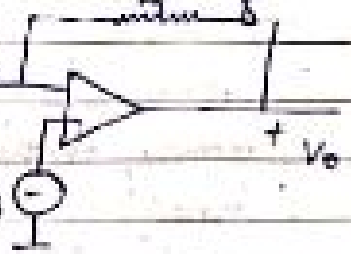
$$\Rightarrow V_o = -I_s R_f \Rightarrow \boxed{I_s = -\frac{V_o}{R_f}}$$

From eq. ① and ② we have

$$\frac{V_s}{R_1} = -\frac{V_o}{R_f} \Rightarrow \frac{V_o}{V_s} = -\frac{R_f}{R_1} \Rightarrow \boxed{A_{VS} = -\frac{R_f}{R_1}}$$

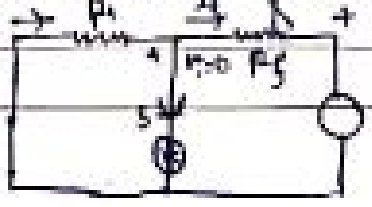
Non-Inverting OPAMP :- If the source is connected to +ve terminal of OPAMP or non-inverting terminal of OPAMP then the OPAMP is called non-inverting OPAMP.

As voltage source is connected to +ve terminal of OPAMP or non-inverting terminal of OPAMP hence OPAMP is called non-inverting OPAMP.



If we consider the OPAMP is ideal then we can implement the condition of short circuit or virtual ground.

The OPAMP after virtual ground can be represented as :-



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From the fig we have $V_s = \frac{R_1}{R_1 + R_f} \times V_o$

$\Rightarrow \frac{V_o}{V_s} = \frac{R_1 + R_f}{R_1}$

$\Rightarrow \frac{V_o}{V_s} = 1 + \frac{R_f}{R_1}$

$\Rightarrow \boxed{A_{V_s} = 1 + \frac{R_f}{R_1}}$

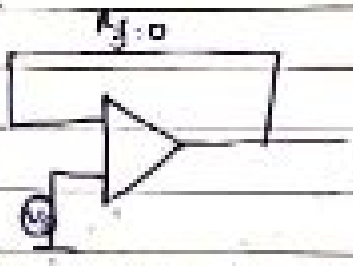
$I_s = \frac{V_o}{R_1 + R_f}$

$V_s = I_s R_1$

$= \frac{V_o}{R_1 + R_f} \times R_1$

NOTE → O/Ulput is non-inverting in nature.

* Voltage Buffer →



As V_s is connected to +ve terminal of OPAMP hence the OPAMP is non-inverting.

$\frac{V_o}{V_s} = 1 + \frac{R_f}{R_1}$

As $R_f = 0$ hence $\frac{V_o}{V_s} = 1 \Rightarrow \boxed{V_o = V_s}$

Application of OPAMP → OPAMP can be used as

* Integrator
* Differentiator
* Summing Amplifier
* Subtractor
* Logarithmic Amplifier
* Exponential Amplifier
* Voltage Buffer

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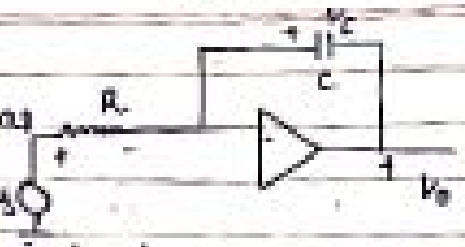
OPAMP as Integrator :-

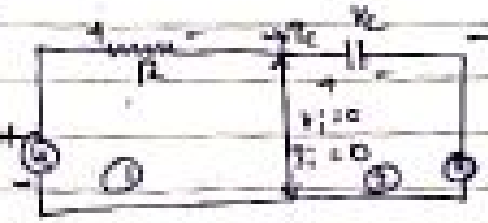
If we consider the OPAMP as ideal OPAMP then we have to apply the concept of virtual ground. So, after applying virtual ground concept the circuit may be described as follows :-



From loop (1) we have :-

$$V_s - I_s R = 0$$

$$\Rightarrow \boxed{I_s = \frac{V_s}{R}} \rightarrow (i)$$



From loop (2) we have :-

$$-V_c - V_o = 0$$

$$\Rightarrow \boxed{V_o = -V_c} \Rightarrow \left(V_o = -\frac{1}{C}\int I_s\, dt\right)$$

$$\Rightarrow V_o = -\frac{1}{C}\int_{t=0}^{t} \frac{V_s}{R}\, dt$$

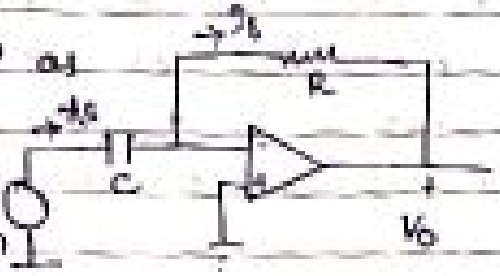
$$\Rightarrow V_o = -\frac{1}{RC}\int_{t=0}^{t} V_s\, dt$$

As output is integration of input hence the OPAMP acts as Integrator.

NOTE :- I_s, V_s, V_o etc are the AC quantities.

OPAMP as Differentiator :-

If we consider the OPAMP as ideal OPAMP then we have to apply the concept of virtual ground & virtual short circuit condition. The OPAMP after applying virtual short circuit condition may be described as follows :-



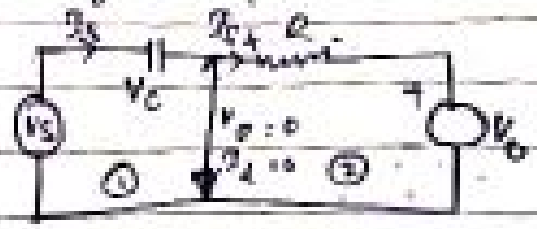
Applying KVL to loop (1)

$$V_s - V_c = 0$$

$$V_s = V_c$$

$$\Rightarrow V_s = \frac{1}{C}\int_{t=0}^{t} I_s\, dt$$

$$\Rightarrow \frac{dV_s}{dt} = \frac{d}{dt}\frac{1}{C}\int_{t=0}^{t} I_s\, dt$$



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$$\Rightarrow \frac{dv_c}{dt} = \frac{1}{C} I_f$$

$$\Rightarrow \boxed{I_f = C \frac{dv_c}{dt}}$$

Applying KVL to loop ②

$$I_f R - V_o = 0$$

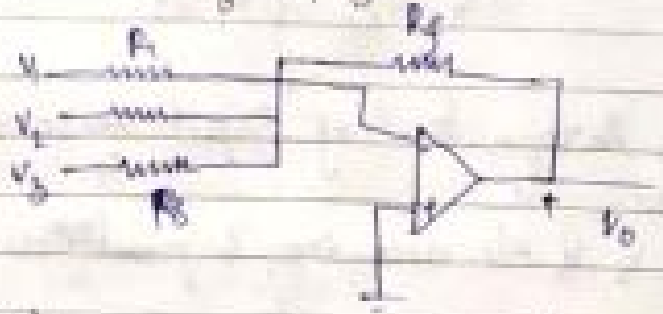
$$\Rightarrow V_o = I_f R$$

$$\Rightarrow \boxed{V_o = -RC \frac{d}{dt} V_i}$$

As the output is ∝ to the derivative of input hence the OPAMP acts as Differentiator.

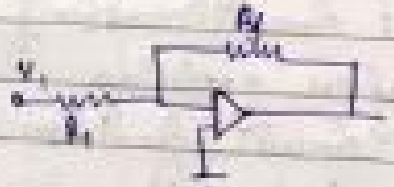
Scaling factor → R_f is known as scaling factor or gain const. Unit → ms

OPAMP As Summing Amplifier →



As resistances are linear element hence they follow superposition principle in an electrical circuit.

Let us consider V_1 as input to the OPAMP, let the output of OPAMP is V_{o1}.



If we $V_{o1} = -\frac{R_f}{R_1} V_1$

Similarly if we apply V_2 as input to OPAMP we will get output as V_{o2}

Mathematically, $\boxed{V_{o2} = -\frac{R_f}{R_2} V_2}$

$$\Rightarrow \boxed{V_{o3} = -\frac{R_f}{R_3} V_3}$$

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Applying superposition theorem we have :-

$$V_o = V_{o1} + V_{o2} + V_{o3}$$

$$\Rightarrow V_o = -\frac{R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2 - \frac{R_f}{R_3} V_3$$

If $R_{eq} = R_1 = R_2 = R_3$ then we have :-

$$V_o = -\frac{R_f}{R} V_1 - \frac{R_f}{R} V_2 - \frac{R_f}{R} V_3$$

$$\Rightarrow \boxed{V_o = -\frac{R_f}{R}\left[V_1 + V_2 + V_3\right]}$$

If $R_f = R$, $V_o = -(V_1 + V_2 + V_3)$

Q) Calculate the CMRR for the circuit measurement $V_1 = 1mV$, $V_o = 120\,mV$ and $V_c = 1mV$ and $V_o = 20\mu V$

$$A_c = \frac{V_o}{V_c} = \frac{20\mu V}{1mV} = \frac{20\times10^{-6}\ V}{1\times10^{-3}\ V} = 20\times10^{-3}$$

$$A_d = \frac{V_o}{V_d} = \frac{120mV}{1mV} = 120$$

$$CMRR = 20\log_{10}\left|\frac{A_d}{A_c}\right| = 20\log_{10}\frac{120}{20\times10^{-3}}$$

$$= 20\log_{10}6000 = 20\log_{10}3 + 20\log_{10}2^2 + 60\log_{10}10$$

$$= 75.44\ dB$$

Slew Rate :- It's defined as the max rate at which the output of the operational amplifier can change in V/μs

$$\boxed{SR = \frac{\Delta V_o}{\Delta t}}\ \frac{V}{\mu sec}$$

Q) It's experimentally found that for an inverting opamp output voltage changes from 8V to 11V when time changes from 3 milli sec to 6 milli sec. Calculate slew rate

$\Delta V_o = 11 - 8 = 3V$

$\Delta t = 6ms - 3ms = 3ms = 3\times10^{-3}$ milli sec

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Similarly, $V_{CE} = V_{CC}$

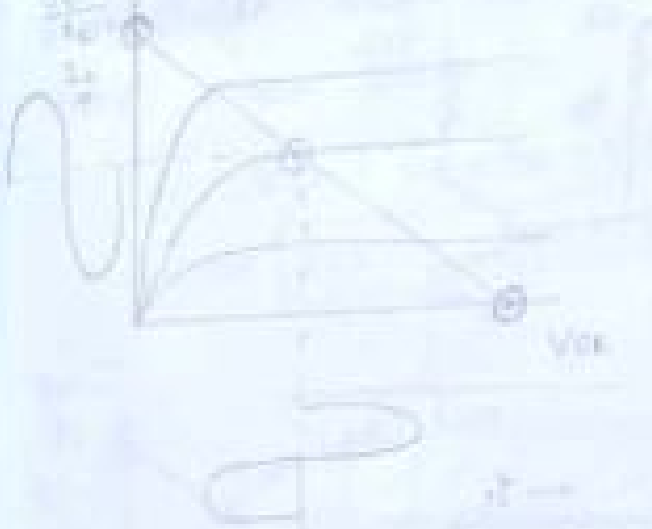
24th Oct, 2019

Note:-

Transistor Biasing -

Biasing is a technique in which stable operating point or q-point must be achieved by using DC - voltages (battery) and resistances for which faithful amplification is possible.

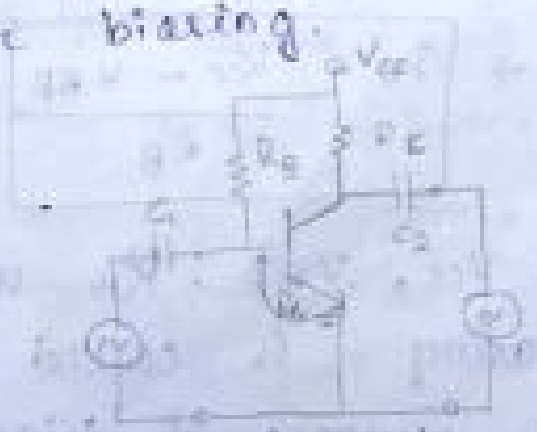
→ After setting q point, we have to apply AC signal as the input at the q point to achieve amplification.



- Types of biasing :-

Taking the resistance and battery into consideration, biasing may be classified as

i) Fixed biasing
ii) Self or emitter biasing
iii) Potential divider biasing or
Voltage divider biasing.



i) Fixed biasing -

→ As biasing refers to DC analysis hence, $f = 0$.

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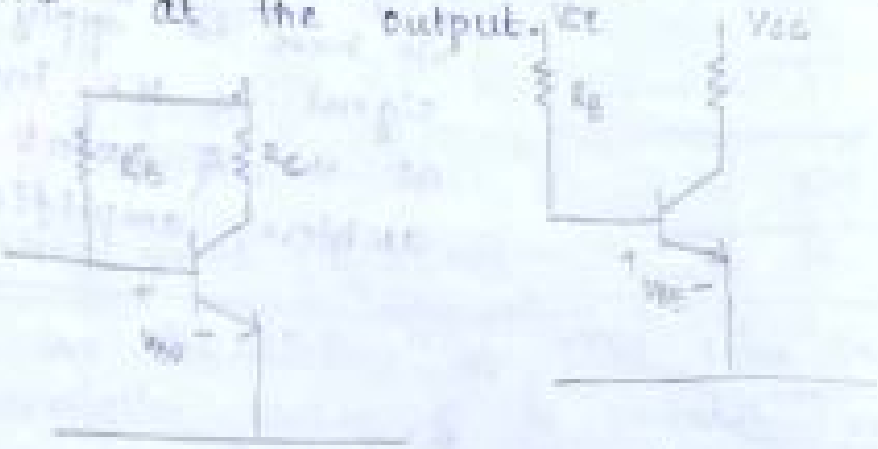
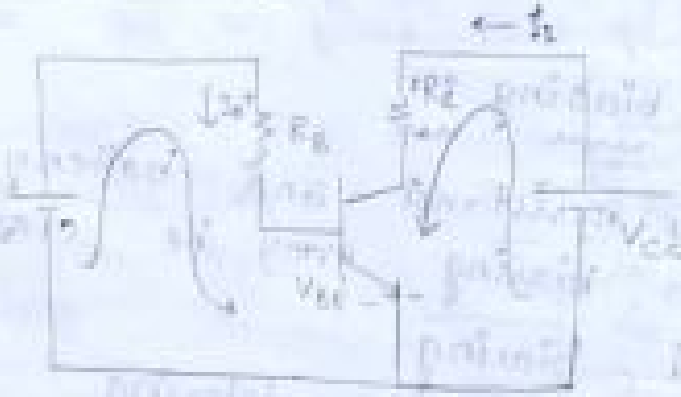
$\Rightarrow X_C = \frac{1}{2\pi f C}$

$= \frac{1}{2\pi \times 0 \times C} = \infty$.

As reactance of the capacitor is ∞, current through the capacitors are zero, it behaves as open circuit.

Hence, no input AC signal is fed to the transistor. Similarly, no output ac signal is collected at the output.





$+V_{CC} - I_B R_B - V_{BE} = 0$

$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$

$\rightarrow$ As V_{CC}, V_{BE}, R_B are fixed, hence the biasing is called as fixed biasing.

$\rightarrow$ The purpose of biasing is to locate a value of base current, so the biasing circuit

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Current I_B may be treated as the best biasing.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Potential diff is independent of path followed.
Higher potential → Lower potential

$R_E = 0$

$\Rightarrow I_E R_E = 0$

$\Rightarrow V_E = 0$

We know, $V_{BE} = V_B - V_E$

$\Rightarrow \boxed{V_{BE} = V_B}$

Applying KVL to the collector - emitter side loop, we have,

$$V_{CC} - I_C \cdot R_C - V_{CE} = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C R_C}$$

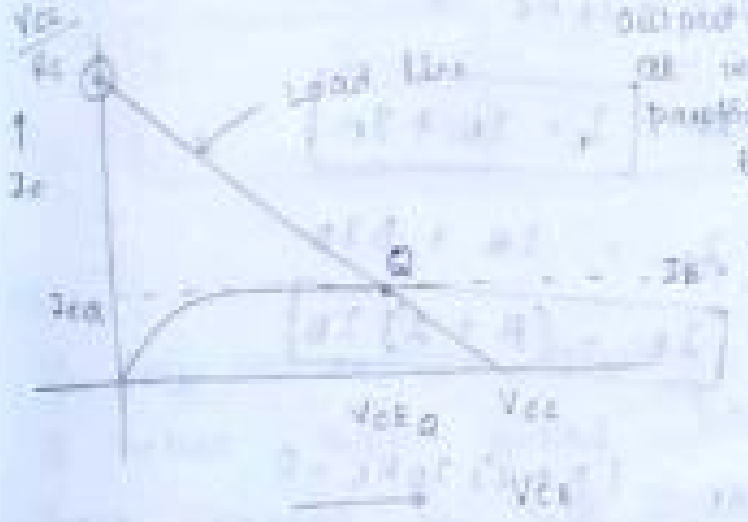
Let, $V_{CE} = 0$

$\Rightarrow V_{CC} = I_C R_C$

$\Rightarrow I_C = \frac{V_{CC}}{R_C}$

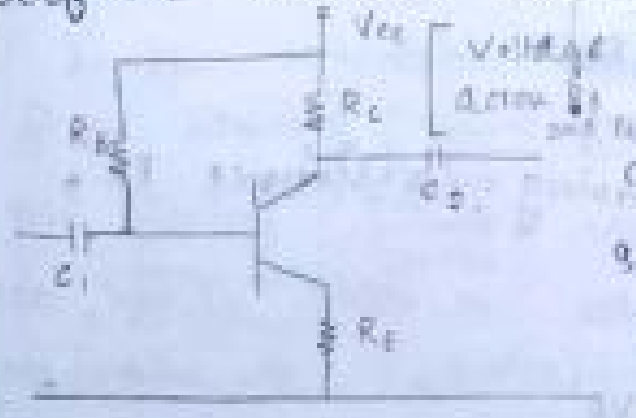
Let $I_C = 0$

$\Rightarrow V_{CE} = V_{CC}$



{DC - open, AC - short}

3) Self or Emitter Biasing -



Voltage across R_E

As the analysis is dc Analysis hence, $f = 0$.

So, the capacitors C_1 & C_2 blocks the ac input & ac output.

So, the capacitor C_1 & C_2 behaves as open circuit.

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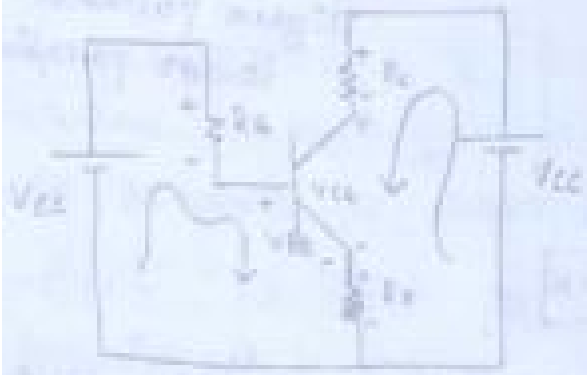
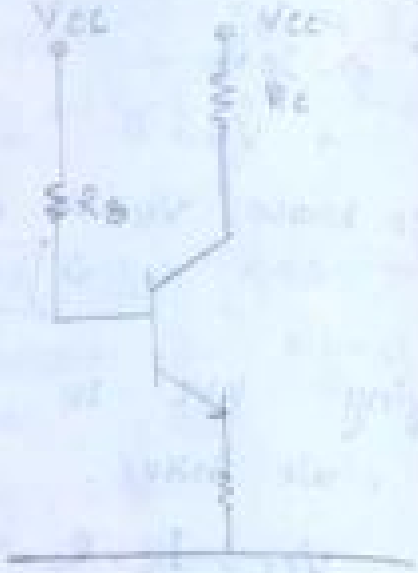
As R_B and R_C are parallel, hence the voltage developed across R_B and R_E are equal.





Applying KVL to base emitter loop, we have

$$+V_{cc} - I_B R_B - V_{BE} - I_E R_E = 0$$

In active region, $\boxed{I_E = I_B + I_C}$

$$\Rightarrow I_E = I_B + \beta I_B$$

$$\Rightarrow \boxed{I_E = (\beta + 1) I_B}$$

$$\Rightarrow V_{cc} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\rightarrow \boxed{I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_E}}$$

As emitter is having resistance R_E,

$$\boxed{V_E = I_E R_E}$$

To find max. current & voltage - current

We know, $V_{BE} = V_B - V_E$

$$\Rightarrow \boxed{V_B = V_{BE} + V_E}$$

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Applying KVL to the common emitter loop we have,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

As collector emitter loop is mainly used to plot load line hence, we have to assume that

$I_B \approx 0$

$\Rightarrow I_C \approx I_E$

$$\Rightarrow V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$\Rightarrow \boxed{V_{CC} - I_C (R_C + R_E) = V_{CE}}$$

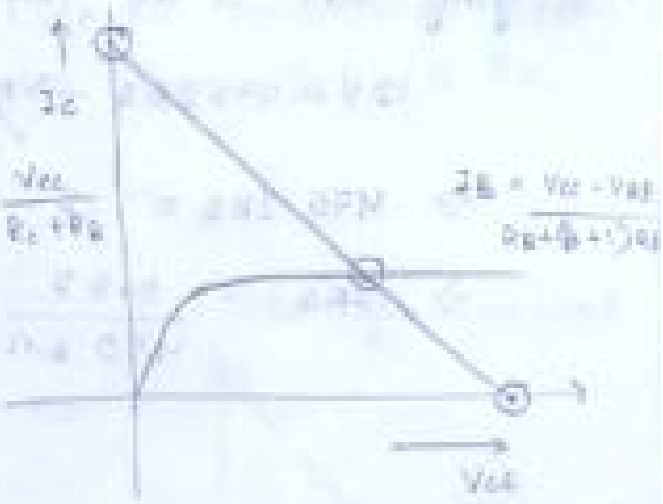
If $I_C = 0$

$\Rightarrow V_{CE} = V_{CC}$

If $V_{CE} = 0$,

$V_{CC} = I_C (R_C + R_E)$

$$\Rightarrow \boxed{I_C = \frac{V_{CC}}{R_C + R_E}}$$



Note :

i) Self or emitter biasing is a better biasing & better than fixed biasing because the base current in self biasing is less than, as compared to fixed biasing.

ii) As the saturation collector current in case of fixed biasing $\left(\frac{V_{CC}}{R_C}\right)$ is greater than that of self biasing $\left(\frac{V_{CC}}{R_C + R_E}\right)$ hence, the fixed biasing can handle maximum collector current. for same value of V_{CE} (V_{CC}).

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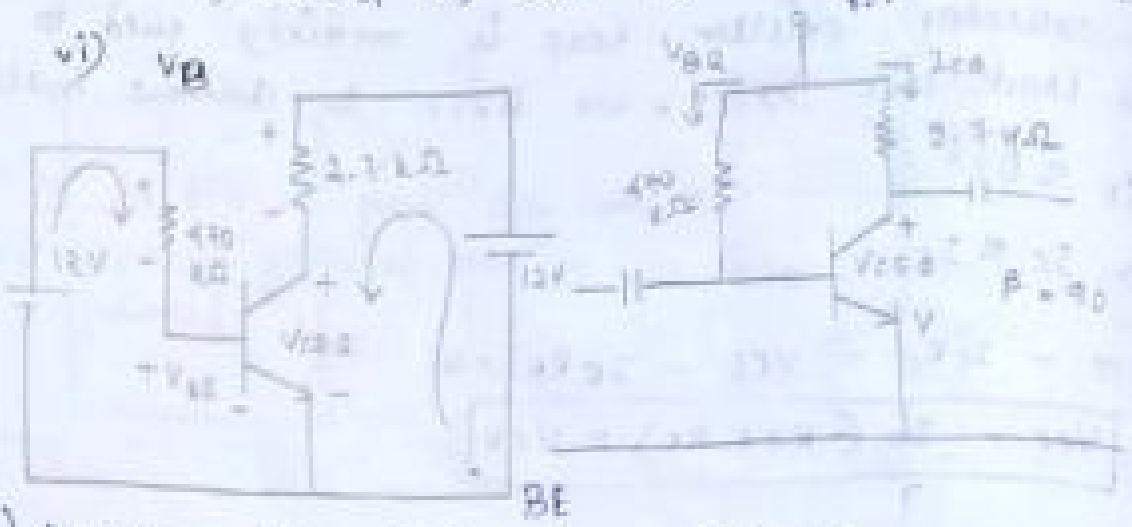
Q. For the fixed bias configuration given the following figure, determine

i) I_{BQ} ii) I_{CQ} iii) V_{CEQ} iv) V_E v) V_C vi) V_B



i) Applying KVL to the loop, we have,

$$12V - 470\,I_{BQ} - V_{BEQ} - 0.7V = 0$$

$$\Rightarrow 470\,I_{BQ} = 12 - 0.7$$

$$\Rightarrow I_{BQ} = \frac{11.3V}{470\,k\Omega} = \frac{0.024}{1000}\,A = 0.024\,mA$$

$$= 0.024 \times 10^{-3} \times 10^{3}\,\mu A$$

$$= \frac{0.024}{1000} \times 10^{6}\,\mu A$$

$$= 24\,\mu A$$

ii) We know that in active region,

$$I_C = \beta I_B$$

$$\Rightarrow \boxed{I_{CQ} = \beta I_{BQ}}$$

$$\Rightarrow I_{CQ} = 24\,\mu A \times 90$$

$$= 2160\,\mu A$$

$$= 2.16\,mA$$

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iii) Applying KVL to the collector - emitter loop, we have

$$+12V - 2.7\,k\Omega\, I_{CQ} - V_{CEQ} = 0$$

$$\Rightarrow V_{CEQ} = 12V - 2.7k\Omega \times I_{CQ}$$

$$\Rightarrow V_{CEQ} = 12V - 2.7k\Omega \times 3.16\,mA$$

$$= 12 - 2.7 \times 10^{3}\,\Omega \times 3.16 \times 10^{-3}\,A$$

$$= 12 - 2.7\,\Omega \times 3.16$$

$$= 12 - 5.53\,V$$

$$= 6.17\,V$$

iv)

→ V_E is 0, as there is no resistance across the emitter, Hence, $R_E = 0$ then $I_B R_E = 0$ So,

$$\boxed{V_E = 0}$$

→ v) $V_{BE} = V_B - V_E$

$$\Rightarrow V_{BE} = 0.7V - V_B$$

$$V_B = I_B R_B$$

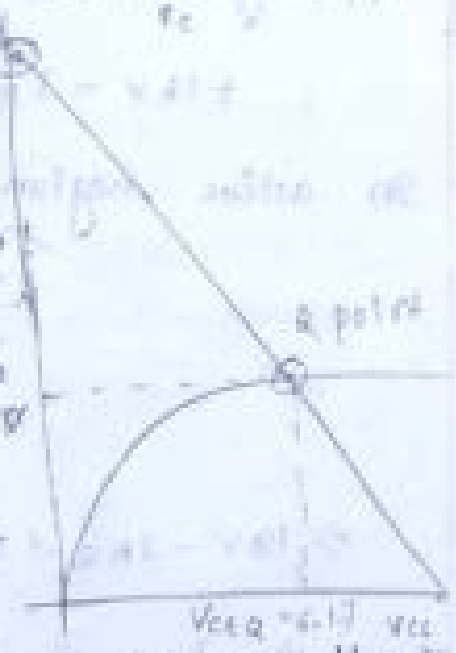
$$= 24 \times 10^{-6} \times 470 \times 10^{3}$$

$$= 11280 \times 10^{-3}$$

$$= 11.28\,V$$

vi) $V_E = V_{CEQ}$

$$\Rightarrow V_E = 6.17\,V$$



Q. Draw the load line of the above question and identify the operating point:-

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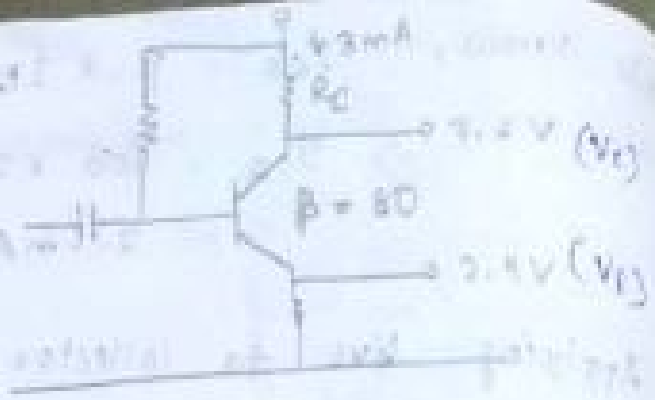
Q2. find :-



a) R_C

b) R_E

c) R_B

d) V_{CE}

a) V_B of the following biasing circuit.

We know, in active region,

$$\boxed{I_C \approx I_E}$$

$$\Rightarrow I_E \approx 3mA$$

As $I_C = \beta I_B$

$$\Rightarrow I_B = \frac{I_C}{\beta} = \frac{3mA}{80}$$

$$\Rightarrow I_B = 0.0375\ mA$$

$$= 37.5\ mA$$

a) Applying KVL to the output loop, we have,

$$+12V - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow 12V - I_C R_C - (V_C - V_E) - V_E = 0$$

$$\Rightarrow 12V - I_C R_C - V_C + V_E - V_E = 0$$

$$\Rightarrow V_C R_C = 12V - V_C$$

$$\Rightarrow 3mA \times R_C = 12V - 4.4V$$

$$\Rightarrow R_C = \frac{4.4V}{3mA}$$

b) $V_E = I_E R_E$

$$\Rightarrow R_E = \frac{V_E}{I_E}$$

$$= \frac{2.4V}{3mA} = 0.8\ k\Omega$$

c) Applying KVL to the input loop, we have,

$$+12V - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\Rightarrow 12V - I_B R_B - 0.7 - 2.4V = 0$$

$$\Rightarrow I_B R_B = 12V - 0.7V - 2.4V$$

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$\Rightarrow R_B = \frac{8.4V}{33.5\,\mu A}$

$= \frac{0.2373}{10^{-6}}\,\Omega$ $\qquad R_B = 237.3\,k\Omega$

$= 0.2373 \times 10^{6}\,\Omega$

d) $V_{CE} = V_C - V_E$

$= 3.6V - 2.4V$

$= 5.2\,V$

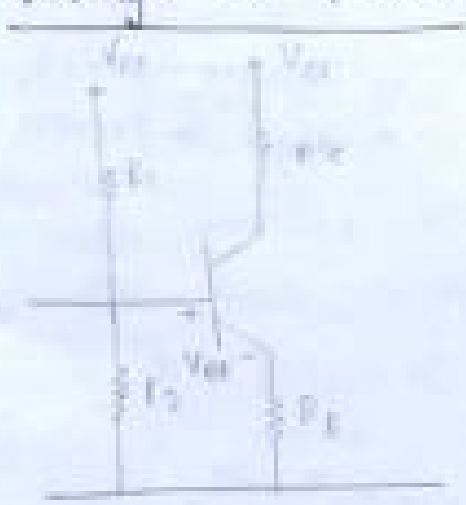
e) $V_{BE} = V_{BE} + V_E$

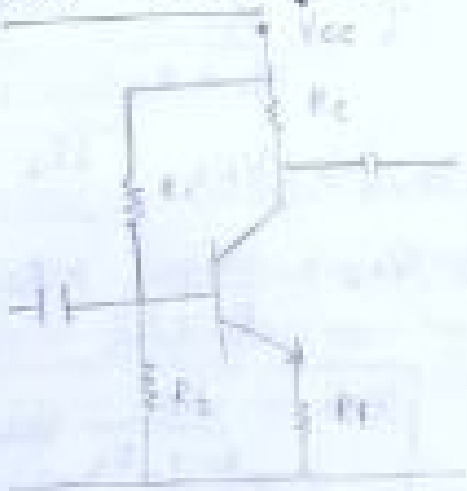
$= 0.7 + 2.4V$

$= 3.1\,V.$

- 5 Nov 2019

Voltage or Potential Divider Biasing :-





i) In the arrangement is a potential divider biasing steps in order to calculate base current we need voltage developed across base and emitter and resistance in the input So, we have to apply thevenins theorem.

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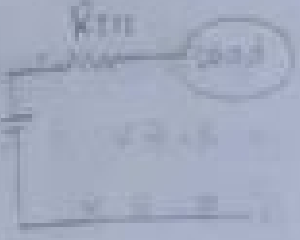
Thevenins Theorem - In a complex circuit, the theorem states that Thevenins voltage, thevenin resistance and load resistance are in series.



$$V_{TH} = V_{R_2}$$

Current in the voltage divider circuit is given by

$$I = \frac{V_{cc}}{R_1 + R_2}$$

source - series
load side - Parallel

$$\text{So, } \Rightarrow V_{R_2} = IR_2$$

$$\Rightarrow V_{R_2} = \frac{V_{cc}}{R_1 + R_2} \times R_2$$

$$\Rightarrow \boxed{V_{TH} = \frac{R_2}{R_1 + R_2} V_{cc}}$$

Calculation of R_{TH} :-

When we calculate R_{TH} we have to put $V_{cc} = 0$, and calculate the resistance developed from the load side.

$$\boxed{R_{TH} = R_1 \parallel R_2}$$

So, according to thevenins theorem,

V_{TH}, R_{TH} and transistor (load) are in series

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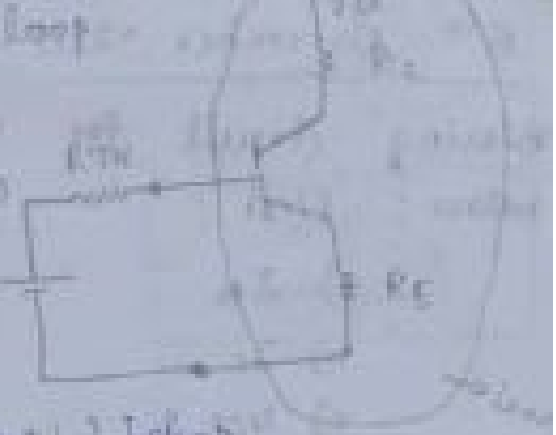
Applying KVL in the input loop

we have

$$+V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$



We know,

$$I_E = (\beta + 1) I_B$$

$$\Rightarrow V_{TH} - I_B R_{TH} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\Rightarrow \boxed{I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}}$$

Applying KVL in the output loop we

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

As $I_E \approx I_C$

hence

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

Note :-

Voltage divider biasing with emitter bias is the best biasing because due to the complementary action of potential divider arrangement the voltage developed across the base and emitter remains as a result base current remains

$$\boxed{I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}} \rightarrow$$

Potential divider biasing

$V_{TH} < V_{CC}$

$\Rightarrow$ attenuator is R_{TH}

For self biasing :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

As R_{TH} is nearly equal to R_B and $V_{TH} < V_{CC}$. Hence voltage divider biasing with emitter resistance is better in compare to self biasing.

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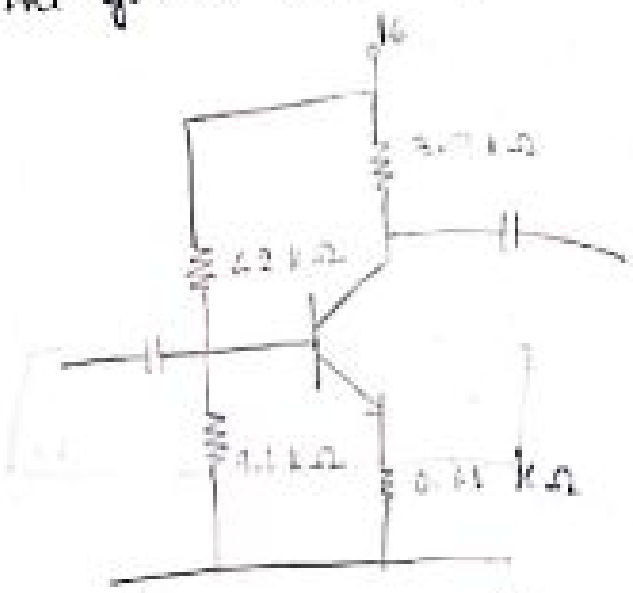
8th November, 2019

Biasing circuit for the voltage divider circuit given below :- Find :

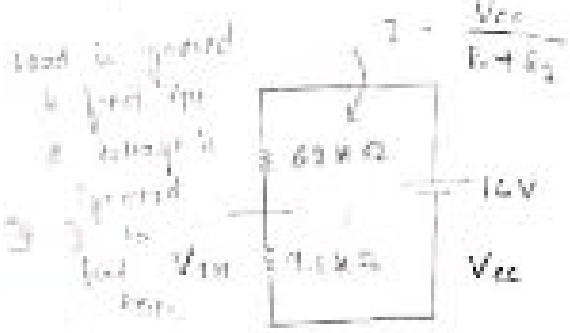
a) I_B
b) I_C
c) V_{CE}
d) V_E
e) V_C
f) V_B.



Answers

$$V_{TH} = \frac{9.1\,k\Omega}{62 + 9.1} \times 16$$

$$= 2.047\ V$$



Calculation of R_{TH} :-

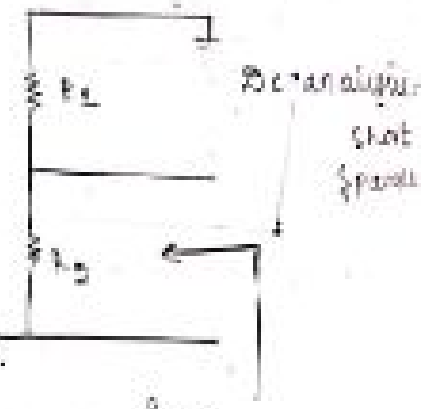
To calculate R_{TH}, we have to short the voltage source (ignore voltage).

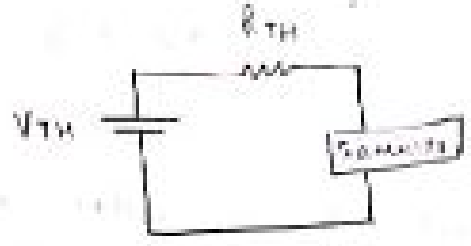
$$R_{TH} = R_1 \parallel R_2$$

$$= \frac{R_1 R_2}{R_1 + R_2}$$

$$= \frac{62 \times 9.1}{62 + 9.1}$$

$$= \frac{564.2}{71.1} = 7.935\ k\Omega$$





P - 80

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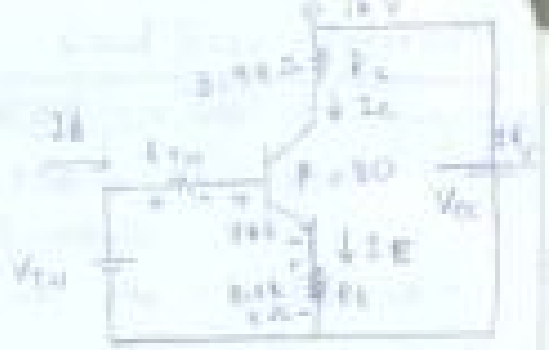
i) $I_B = \dfrac{V_{TH} - V_{BE}}{R_{TH} + (\beta+1)R_E}$

$= \dfrac{2.044\,V - 0.7\,V}{3.9\,k\Omega + 81 \times 0.68\,k\Omega}$

$= \dfrac{1.344\,V}{63.018\,k\Omega}$

$= 0.0213\,mA = 0.0213 \times 10^{-3}\,A$

$\Rightarrow \boxed{I_B = 21.3\,\mu A}$



ii) $I_C = \beta I_B$

$= 80 \times 0.0213\,mA$

$= 80 \times 21.3\,\mu A$

$= 1704\,\mu A$

$\Rightarrow \boxed{I_C = 1.7\,mA}$

iii) $V_{CE} = V_{CC} - I_C(R_C + R_E)$

$\Rightarrow V_{CE} = 12\,V - 1.7\,mA\,(3.9\,k\Omega + 0.68\,k\Omega)$

$\Rightarrow \boxed{V_{CE} = 8.214\,V}$

iv) $V_E = I_E R_E$

$\Rightarrow V_E = 1.7\,mA \times 0.6\,k\Omega$

$\Rightarrow \boxed{V_E = 1.156\,V}$

v) V_C, voltage across collector.

$V_{CE} = V_C - V_E$

$V_C = V_{CE} + V_E$

$\Rightarrow V_C = 8.214 + 1.156$

$\Rightarrow \boxed{V_C = 9.37\,V}$

vi) $V_B = V_{BE} + V_E$

$= 0.7\,V + 1.156$

$\Rightarrow \boxed{V_B = 1.856\,V}$

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Collector feed back biasing

Applying KVL to the B-E loop,

$$+V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\Rightarrow V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$$

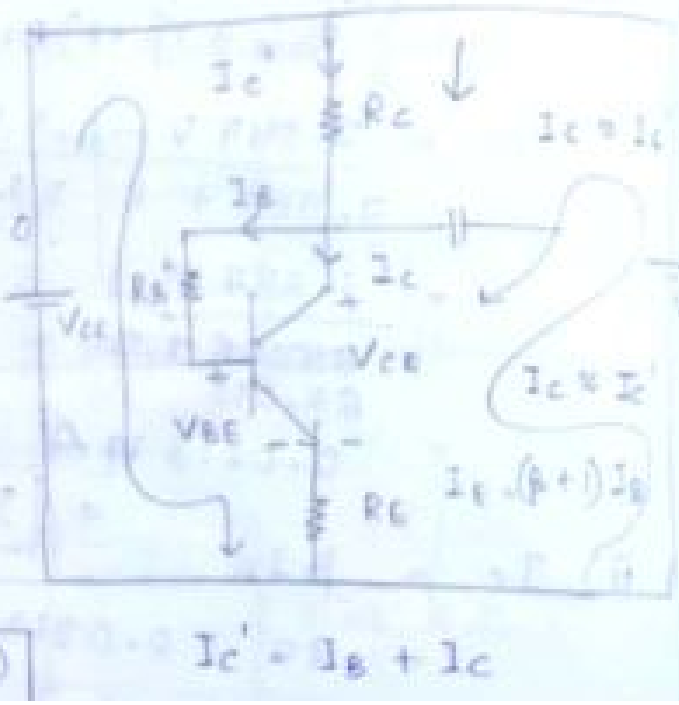
$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{\beta R_C + R_B + (\beta+1) R_E}$$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}}$$

As $I_C \approx I_E$, then,

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$



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CLIPPERS and CLAMPERS

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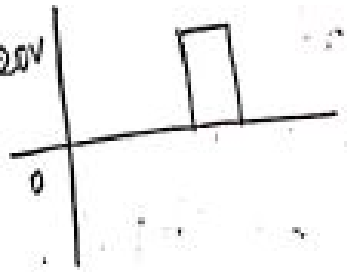
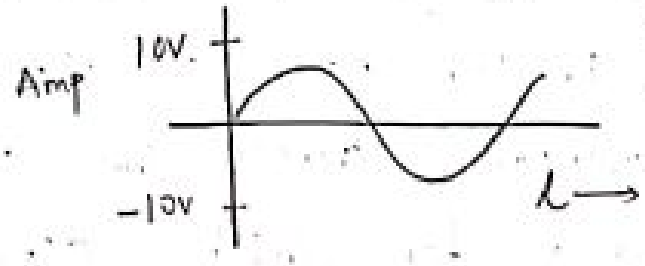
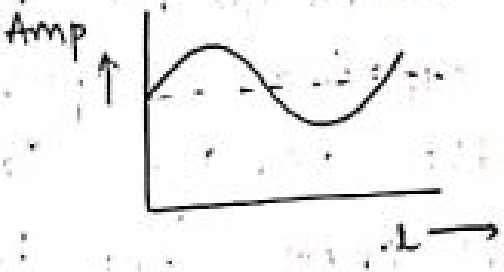
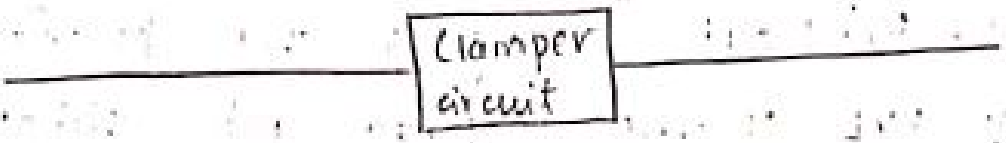
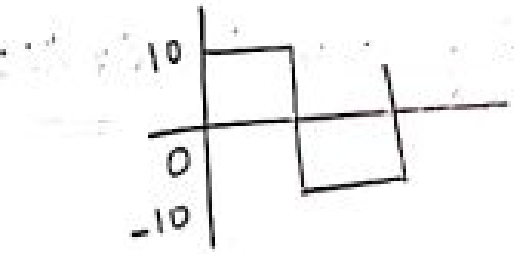
Clampers.

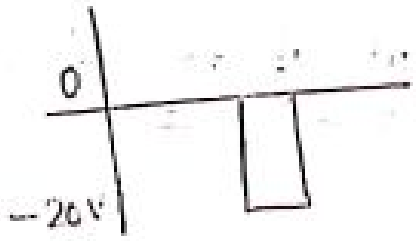


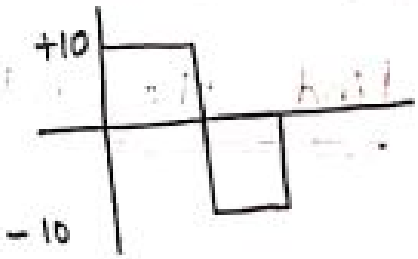






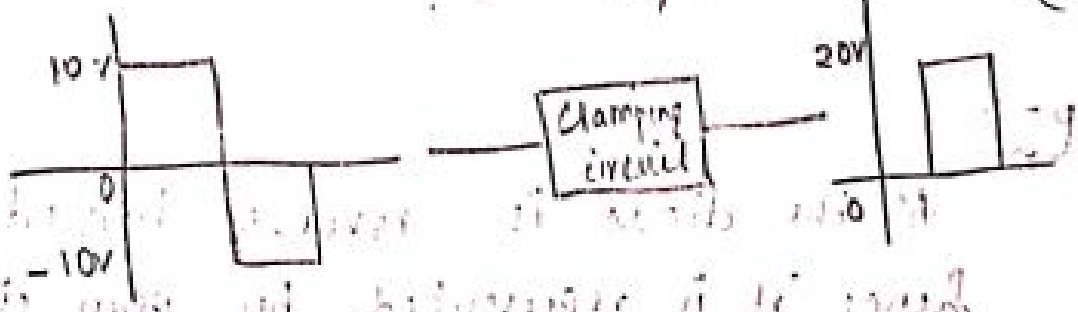






Clamping circuits are the circuits which are require to change the dc level of a signal without affecti ng the dynamic range or shape of the input sign Clamping maybe classified as :-

i) Positive clamping - If the dc level of- an input signal shifts to a positive amplitude then the clamping is said to be positive clamping.



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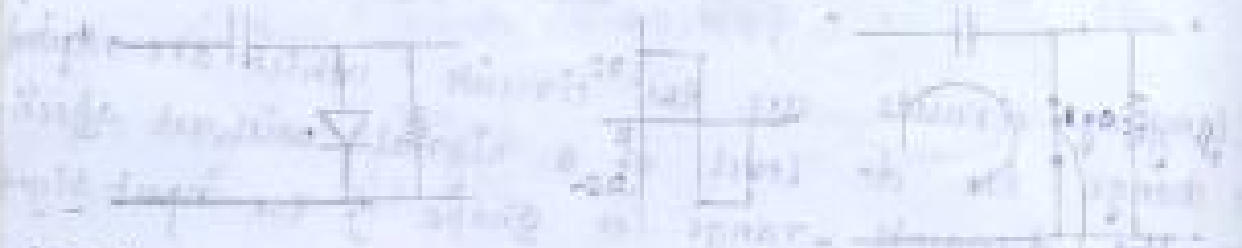
(ii) Negative clamping :- If the dc level of an input signal shifts to -ve amplitude then the clamping is called -ve clamping.

Procedure to solve clamping circuit :-

i) check the input for which diode is forward bias. As the bias in forward bias then the capacitor charges to the peak value. So, calculate the voltage developed across the capacitor.

ii) Check the input for which diode is reverse bias. Without changing the polarity in step (i) apply KVL to the loop to get output voltage.

(Q.1) Find the output of the following clamping circuit



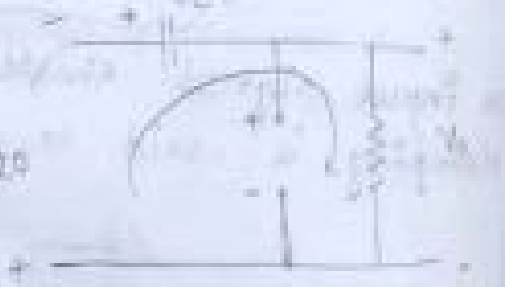
Step - 1

Applying KVL to the loop.

$$+20\,V - V_c - 0 = 0$$

$$V_c = 20\,V$$

$$V_0 = 0$$



Step - 2

At the diode is reverse biased in -ve half since it is represented by open circuit.

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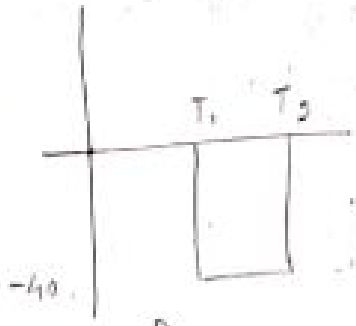
$-20 - V_C - V_o = 0$

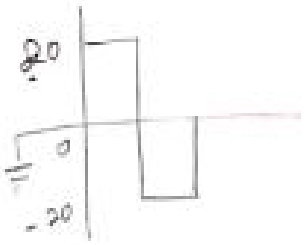
$\Rightarrow V_o = -20 + V_C$

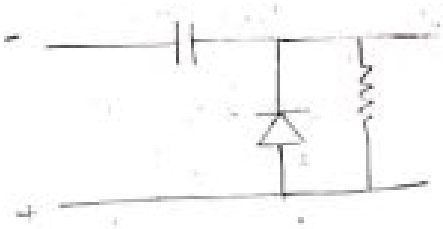
$\Rightarrow V_o = \cancel{(-20+20)} -20 - 20$

$\Rightarrow \boxed{V_o = -40\ V}$



Q. Find the output of the following clamping circuit:

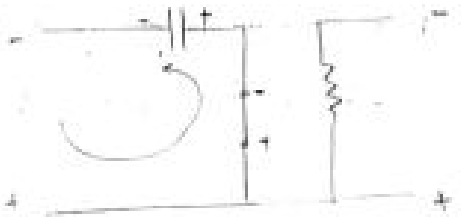




$+20 - 0 - V_C = 0$

$\Rightarrow \boxed{V_C = 20\ V}$

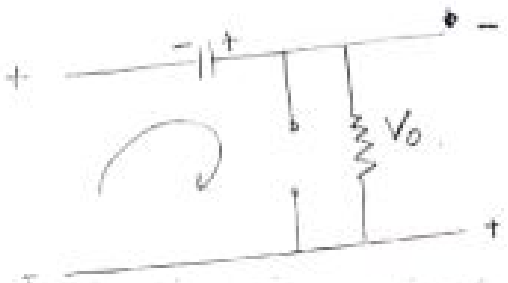
$\Rightarrow \boxed{V_o = 0V}$



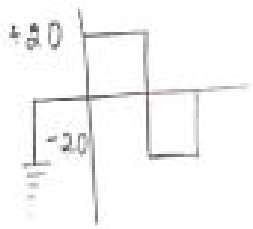
$+20 + V_C + V_o = 0$

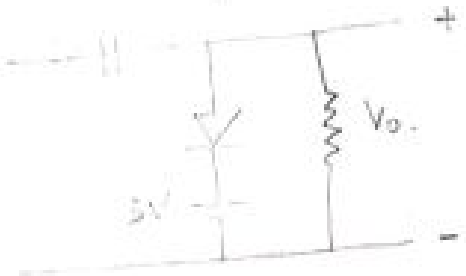
$\Rightarrow V_o = -20 - 20$

$\Rightarrow \boxed{V_o = -40\ V}$



Q. Find the output of the following clamping circuit :-





(i) We have to calculate voltage across the capacitor when the diode is forward bias. As, for positive half of the input cycle diode is forward bias and capacitor charges.

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(i) Applying KVL to the loop we have

$+20 - V_c - 5 = 0$.

$\boxed{V_c = 15\ V}$

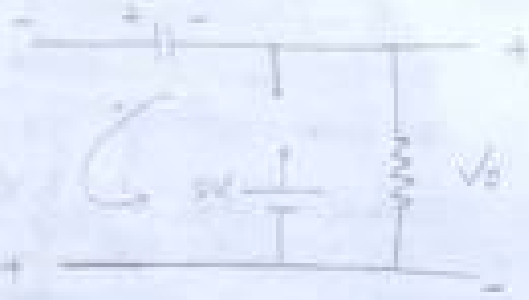
(ii) We have to find the output voltage V_o to the +ve half of the input cycle.

Applying KVL to the loop 2:-

$+5 + V_o = 0$

$\Rightarrow \boxed{V_o = 5}$

(iii) For -ve half of the input cycle, diode is reverse biased. Hence, get open circuit (Polarity of previous circuit is not changed)

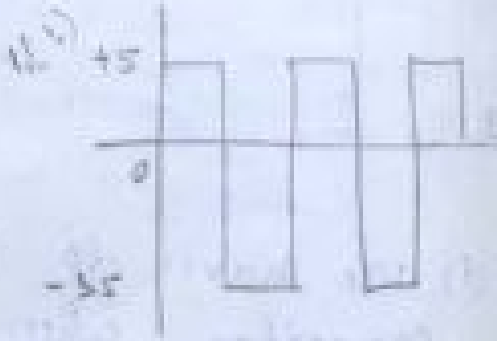


(iv) Applying KVL to the loop, we have

$+20\ V + V_o + V_c = 0$

$\Rightarrow V_o = -20 - 15$

$= -35\ V$.



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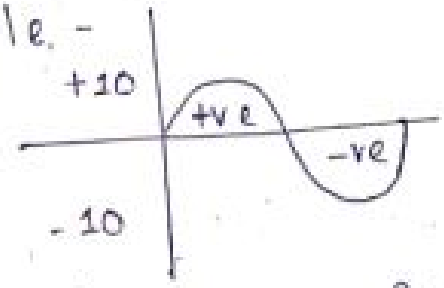
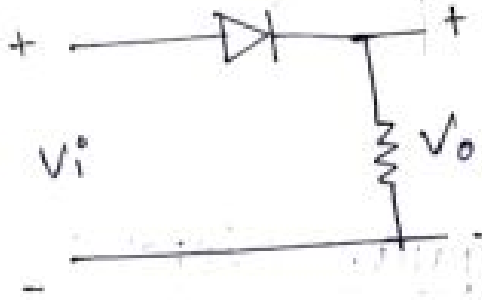
• Clipping - Clipping is a technique in which some portion of the input ~~waveform~~ waveform is clipped.

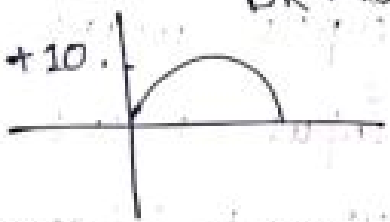
→ The dynamic range in clipping circuit are not maintained.

Example -



Dynamic range = 20.





→ A clipper may be classified as :-

a) Series clipper - If the output is collected across the load then the clipper is called series

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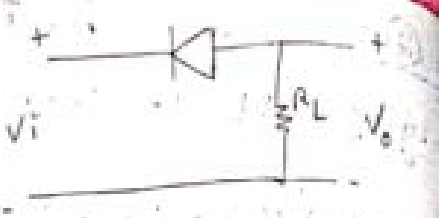
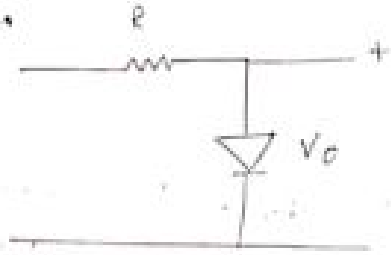
clipper.

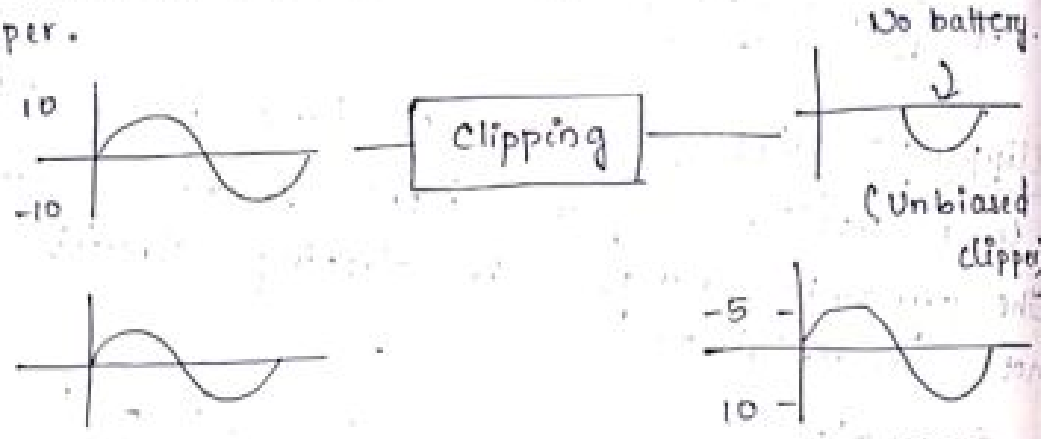


b) Parallel / Shunt clipper -
If the output is collected across the diode, then the clipper is called as parallel clipper.

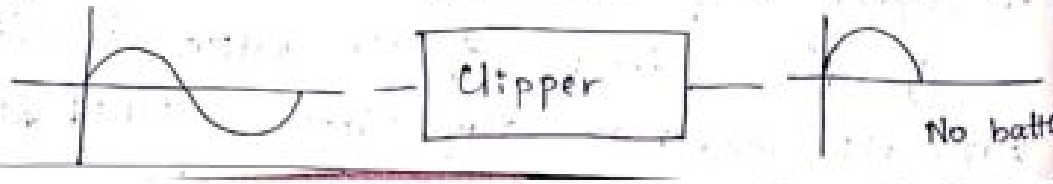


• By taking the input / source, the clipper can be classified as :

a) Positive clipper - If +ve half of any portion of the +ve half of the input wave form is clipped, then the clipper is called +ve clipper.



ii) Negative clipper : If -ve half of any of the input wave form or some portion of the input wave-form of a clipper circuit is clipped. Then, the clipper is called -ve clipper.



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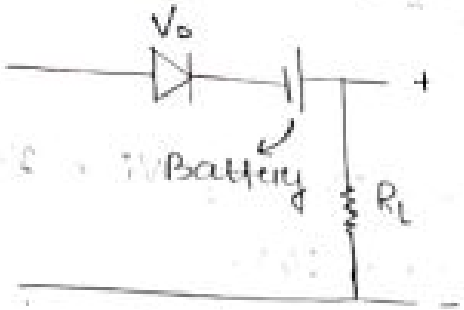
With battery
(Biased clipper)

Biased clipper :-

A clipper is said to be biased clipper, if it contains any battery or other voltage sources.

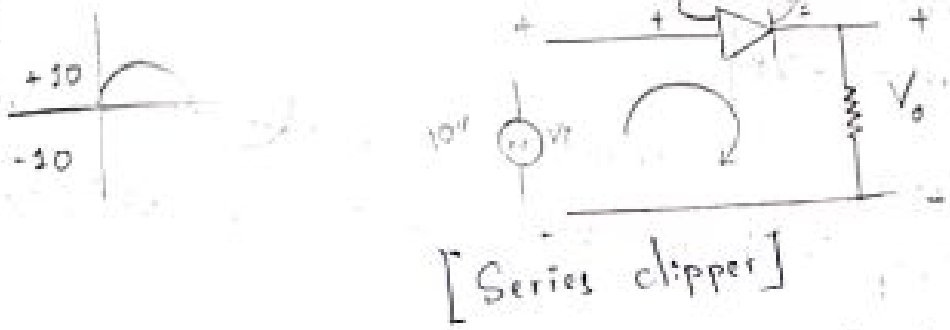


Procedure to solve clipping circuit :-

1. Ignoring the load, find the output across the diode (V_D).
2. If V_D is +ve, then apply KVL to get output.
3. Similarly repeat step 2, to get output voltage if possible.

Q. Find the output of the following clipping circuits :-

1.



[Series clipper]

Assuming $R_L = 0$, the KVL can be written by.

$+ V_i - V_D = 0$

$+ 10 - V_D = 0 \Rightarrow \boxed{V_D = V_i}$

$\Rightarrow \boxed{V_D = 10\,V}$

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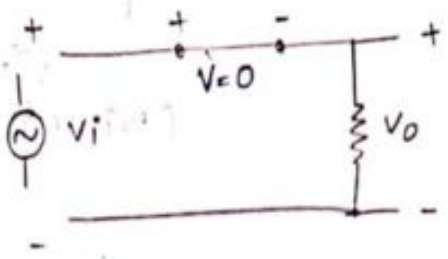
If V_i is +ve, then V_D is +ve, so, the diode is short circuit. (FB)



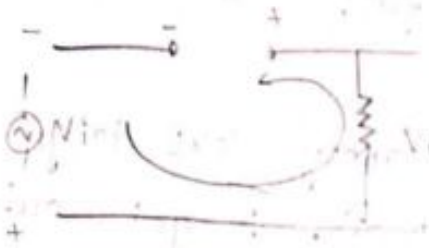
Apply KVL to the loop...

$$V_i - 0 - V_o = 0$$

$$\Rightarrow \boxed{V_i = V_o}$$

If V_i is 0V., $V_o = 0V$, If V_i = 1V, V_o = 1V
If V_i is 10 V, V_o = 10 V..

For -ve half of the input, $V_D = -V_i$, so, the diode is open circuit. (RB)



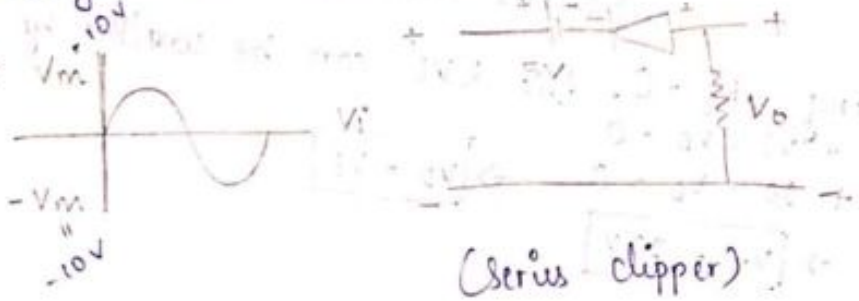
Apply KVL to the loop;

$$-V_i + 0 + -V_o = 0$$

$$\Rightarrow -V_i = V_o$$

$$\Rightarrow \boxed{V_i = -V_o}$$

As the clipper is a series clipper, hence the current through the load is zero. So, the output is zero

Q. 

(Series clipper)

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i) Applying KVL to the loop (without considering the load resistance) we have :-

$$+V_i - 5V + V_D = 0$$

$$\therefore \boxed{V_D = 5 - V_i} \quad \text{---(I)}$$

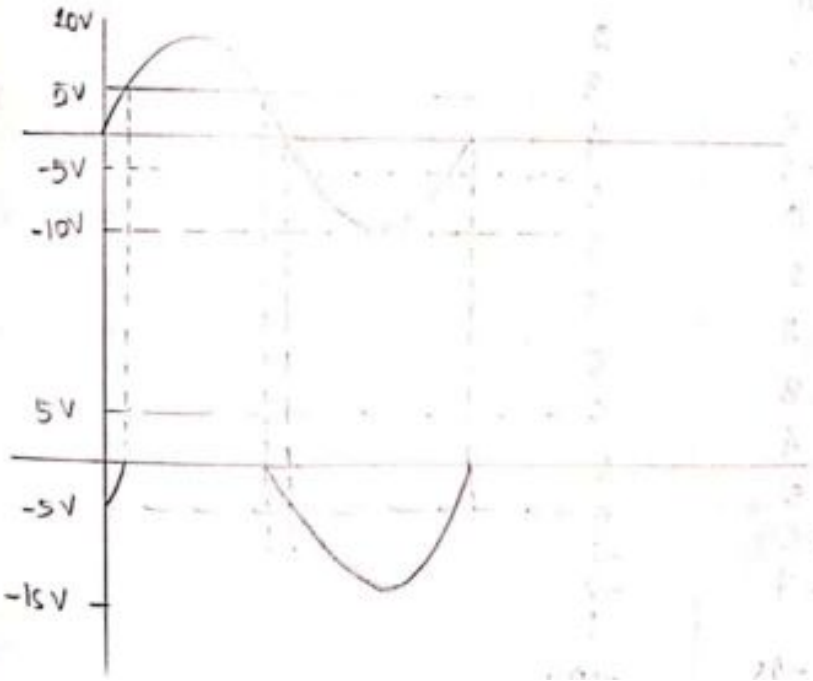
FB - current will flow
RB - doesn't flow

ii) By taking short circuit condition of the diode, if we will apply KVL to the loop, we have.

$$+V_i - 5 - V_o = 0$$

$$\therefore \boxed{V_o = V_i - 5} \quad \text{---(II)}$$

V_i	V_D	V_o
0	5	-5
1	4	-4
2	3	-3
3	2	-2
⋮	⋮	⋮
10	-5	0
-1	6	-6
-2	7	-7
-3	8	-8
⋮	⋮	⋮
-9	14	-14
-10	15	-15



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